1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0001188998	PRODUCTION RELEASED	2011-07-22

J59
(7/22/2011)

DRAWING TITLE: SCH,J59,MLB

Apple Inc.

DRAWING NUMBER: 051-8774 | SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 1 OF 110

SHEET: 1 OF 48

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

J59 BLOCK DIAGRAM

Apple Inc.

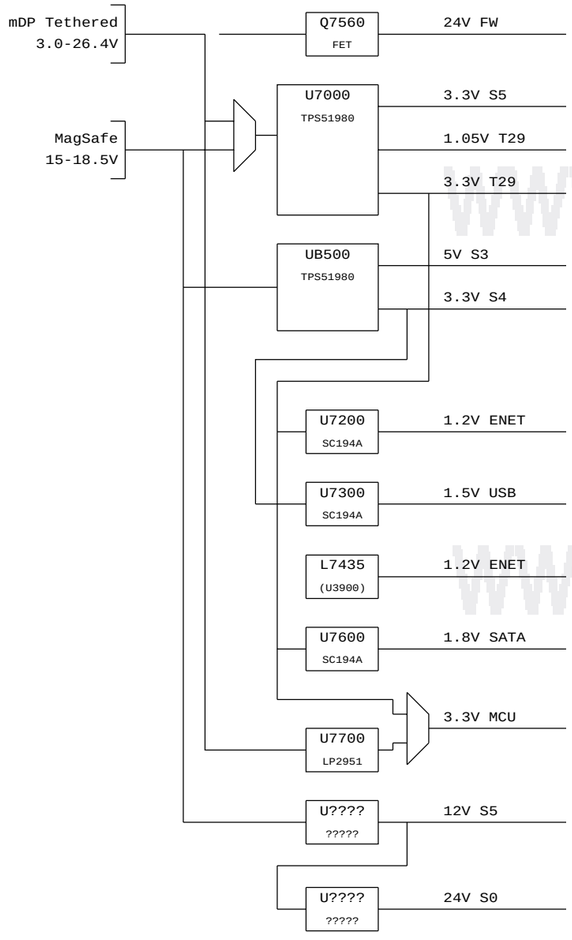
DRAWING NUMBER 051-8774 SIZE D

REVISION C.0.0

BRANCH

PAGE 2 OF 110

SHEET 2 OF 48



Device Function:	Dr.B	Mr.Dev	Mr.Dev	Mr.Dev	Display	ENET	FW	SATA	DPIn
Power Source:	Self	Self	Bus	Bus	Self	Bus	Bus	Bus	Bus
Wake Support:	Yes	Yes	Yes	No	Yes	Yes	No	No	No
24V FW	FW (420mA / 10W)	FW (420mA)	FW (420mA)	FW (420mA)	FW (420mA)	N/A	FW (420mA)	N/A	N/A
3.3V S5	MCU (10mA)	MCU (10mA)	N/A	N/A	MCU (10mA)	N/A	N/A	N/A	N/A
1.05V T29	RTRx2,FW,SATA	RTR,FW,SATA	RTR,FW,SATA	RTR,FW,SATA	RTRx2,FW	RTR	RTR,FW	RTR,SATA	RTR
3.3V T29	RTRx2,FW,SATA	RTR,FW,SATA	RTR,FW,SATA	RTR,FW,SATA	RTRx2,FW	RTR	RTR,FW	RTR,SATA	RTR,mDP
5V S3	USB (2.1A)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
3.3V S4	mDPx2 (1A)	mDPx2 (1A)	N/A	N/A	mDP (1A)	N/A	N/A	N/A	N/A
1.2V ENET	DP++ (440mA)	DP++ (440mA)	N/A	N/A	DP++ (440mA)	N/A	N/A	N/A	N/A
1.5V USB	PLX (USB) (210mA)	PLX (USB) (210mA)	N/A	N/A	PLX (USB) (210mA)	N/A	N/A	N/A	N/A
1.2V ENET	N/A	N/A	ENET (400mA?)	N/A	N/A	ENET (400mA?)	N/A	N/A	N/A
1.8V SATA	SATA (250mA)	SATA (250mA)	SATA (250mA)	SATA (250mA)	N/A	N/A	N/A	SATA (250mA)	N/A
3.3V MCU	N/A	N/A	MCU (10mA)	MCU (10mA)	N/A	MCU (10mA)	MCU (10mA)	MCU (10mA)	MCU (10mA)
12V S5									
24V S0									

T29 Bus-Powered Device Power States:

S4: Device negotiation, SRC_PWR = 3.0-3.6V (MCU function only)
S3: Device sleep, SRC_PWR = 5.0-26.4V (optional wake functions supported)
S0: Device running, SRC_PWR = 21.6-26.4V (run functions supported)

NOTE: Devices not supporting wake function would not implement S3 state.

T29 Self-Powered Device Power States:

S5: Device standby, no cable attached (MCU function & DP port power only)
S3: Device sleep, cable attached (optional wake functions supported)
S0: Device running, cable attached (run functions supported)

DP/T29 Display-Specific Power States:

(In addition to S5-S0 states for T29 Self-Powered Device)
D5: Display standby, no cables attached
D3: Display sleep, DP cable detached or no source power, USB VBus present (USB wake supported)
D2: Display low-power, DP cable attached and source powered, source asleep per AUX command to TCON (USB wake supported)
D0: Display ready, DP cable attached and source powered

NOTEs:
- D5 implies S5, S0 implies D0.
- If only native DP source is attached, any Dx state can be supported while T29 is in S5.

NOTE: D2 not supported on Dr.B as there is no direct connection from panel TCON

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: Power Block Diagram

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 3 OF 110
SHEET: 3 OF 48

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1575	PCBA,MLB,J59	BASIC
085-2422	PCBA,MLB,DEV,J59	DEVELOPMENT

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,T29HV:P12V,BIT_BANG_I2C,ENET_WAKE:PCIE,PIUSB_REV:B,PRODUCTION

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0945	1	IC,T29-PRQ,220 FCBGA,15X15MM	U3600	CRITICAL	
338S0753	1	IC FW643 E 1394B PHY/OHCI LINK/PCI E 12	U4100	CRITICAL	
343S0549	1	IC ASIC GBIT ENET QFN 48 6X6 BCM57761 B0	U3900	CRITICAL	
338S0977	1	PCI EXPRESS TO USB 2 0 HOST CONTROLLER(REV B)	U4600	CRITICAL	

FLASH

	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
RAW: 335S0550	341T0376	1	IC EEPROM J59 PRIMARY SPI 32KBIT MLP8	U3690	CRITICAL	
RAW: 335S0800	341T0331	1	ENET FLASH C IV NO SD J59	U3990	CRITICAL	
RAW: 335S0559	341T0375	1	IC EEPROM FW643 E2 GUID I2C 2KBIT MLP8	U4290	CRITICAL	
RAW: 337S4115	341T0385	1	IC MCU 32B LPC1114 32KB/8KB HVQFN33 J59	U5000	CRITICAL	
RAW: 337S4115	341T0385	1	IC PRGRMD LPC1114 T29 SUPER MCU HVQFN33	U9330	CRITICAL	
RAW: 337S3558	341T0378	1	IC PRGRMD LPC2144 J59 SYSTEM MCU	U2617	CRITICAL	
RAW: 353S2320	341T0369	1	IC PRGRMD PNX0161 AUDIO/HID TFBGA88	U1400	CRITICAL	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0977	376S0859		ALL	DIODESINC ALT FET
376S0972	376S0612		ALL	ROHM ALT FET
377S0107	377S0066		ALL	ON SEMI ALT RCLAMP
155S0431	155S0289		L1204	ALTERNATE CM CHOKE
376S1029	376S0953		ALL	ALTERNATE DC/DC FET
376S1030	376S0801		ALL	ALTERNATE DC/DC FET
376S1017	376S0612		ALL	ALTERNATE TOSH SS FET
377S0124	377S0057		ALL	ALTERNATE VARISTOR
152S1483	152S1376		ALL	ALTERNATE INDUCTOR
155S0691	155S0183		ALL	ALT BEAD FOR BL FILT
128S0262	128S0220		ALL	ADDS KEMET TO SANYO
138S0684	138S0660		ALL	ADDS MURATA TO TAIYO
155S0571	155S0309		ALL	ALTERNATE FERRITE
353S3477	353S3207		ALL	ALTERNATE FAB U9410

Schematic / PCB / EEEE #'s

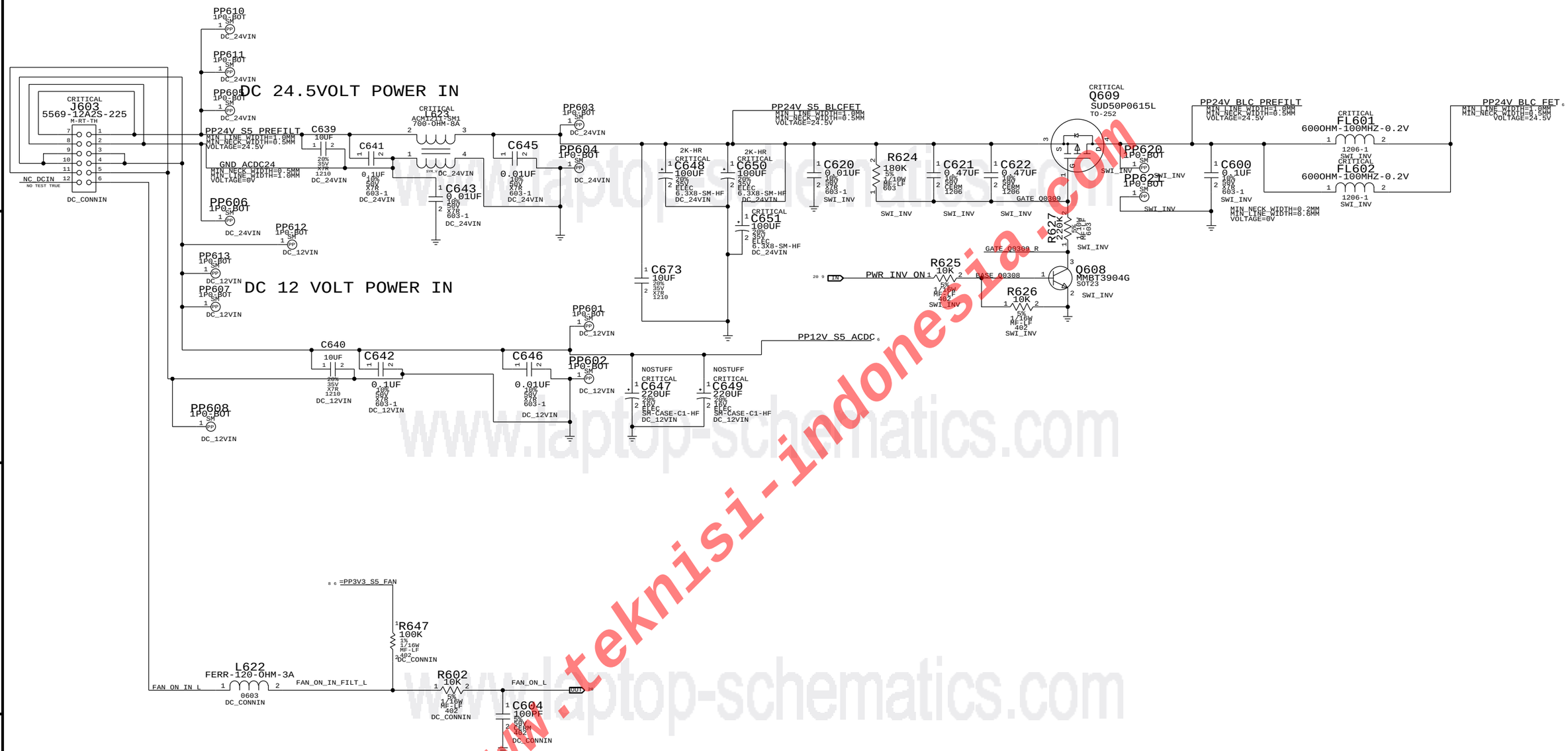
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
820-2997	1	PCBF MLB J59	PCB1	CRITICAL	
051-8774	1	SCH MLB J59	SCH1	CRITICAL	
825-7122	1	MLB LABEL 48 0MM X 4 8MM	[EEEE_DHMY]	CRITICAL	

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
BOM Configuration & Misc

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 4 OF 110
SHEET 4 OF 48



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: DC POWER IN

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 6 OF 110

SHEET: 5 OF 48

S5 Rails

PP12V_S5
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=12V
MAKE BASE=TRUE

PPVIN_SW_T29BST (37) — VOLTAGE=12V

PP12V_S5_ACDC (5)
=PP12V_S5_FANFET (19)
=PP12V_S5_5V3V_VREG (39)
=PP12V_S5_AUDIOFET (19)
=PP12V_S5_LCDFET (19)
=PP12V_S5_P12VS0FET (40)
=PPVIN_SW_T29BST (6 37)

PP5V_S5
MIN LINE WIDTH=0.6 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=5V
MAKE BASE=TRUE

PP5V_S5_REG (39)
=PP5V_S5_USB (33)
=PP5V_S5_AUDIOFET (19)
=PP5V_S5_CAMFET (10)
=PP5V_S5_P1V05S0_VREG (36)

PP3V3_S5
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE BASE=TRUE

PP3V3_S5_REG (39)
=PP3V3_S4_DEVRESET (7)
=PP3V3_S5_FANBUF (19)
=PP3V3_S5_FAN (5 8)
=PP3V3_S5_USB (31 32 33)
=PP3V3_S5_LPC (20 35)
=PP3V3_S5_AUDIOFET (19)
=PP3V3_S5_TCON (21)
=PP3V3_S5_JTAG (11)
=PP3V3_S5_BLC (9)
=PP3V3_S5_ALS (35)
=PP3V3_S5_P3V3S3FET (40)
=PP3V3_S5_P3V3S0FET (40)
=PP3V3_S4_DPAPWRSW (7 43)
=PP3V3_S5_T29P

RT800
0
1 — 2
5% 1/10W MF-LF 603
PP3V3_S4_MCU (MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE BASE=TRUE) = =PP3V3_S4_MCU (11 34)

S0 RAILS

PP24V_S0_BLC
MIN LINE WIDTH=1.0MM
MIN NECK WIDTH=0.5MM
VOLTAGE=24.5V
MAKE BASE=TRUE

PP24V_BLC_FET (5)
=PP24V_BLC_LEDS (9)

PP12V_S0
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=12V
MAKE BASE=TRUE

=PP12V_S0_FET (40)
=PP12V_S0_FW (30)
=PP12V_S0_P1V05S0_VREG (36)

PP3V3_S0
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE BASE=TRUE

=PP3V3_S0_FET (40)
=PP3V3_S0_DEVRESET (7)
=PP3V3_S0_CK505 (22)
=PP3V3_S0_T29P (7 11 23 24)
=PP3V3_S0_I2C_UC (35)
=PP3V3_S0_FWPHY (28 29 30)
=PPVDDIO_S0_T29P_CLK (22)
=PP3V3_S0_TCPWRSW (40 41)
400 mA? =PP3V3_S0_ENET_PHY (20 26)
=PP3V3_S0_TCON (21 35)
=PP3V3_S0_I2C_T29 (35)

PP1V05_S0
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE BASE=TRUE

PP1V05_S0_REG (36)
=PP1V05_S0_CK505 (22)
=PP1V05_S0_T29P (24)

T29 PORT POWER VOLTAGE

1000 MA

PP15VR12V_S3
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=15V
MAKE BASE=TRUE

=PP15V_T29_REG (37)
=PPHV_SW_DPAPWRSW (43) 500 MA

37 6 =PPVIN_SW_T29BST

CRITICAL
T29HV:P12V
R890
0.001
1 — 2
1% 1W MF 0815-HF

T29HV:P12V
R895
0
5% 1/10W MF-LF 402
T29BST_PWREN_DIV_L OUT (37)

750 MA

PP3V3_SW_TCPWR
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE BASE=TRUE

=PP3V3_S0_TCPWR_FET (41)
=PP3V3_S0_TCCONN (41) 750 MA

S3 RAILS

PP3V3_S3
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE BASE=TRUE

< 2100 mA

=PP3V3_S3_FET (40)
=PP3V3_S3_ENET_PHY (20 25)
=PP3V3_S3_USB (7 32 35)
=PP3V3_S3_ENET_SYSCLK (22)
=PP3V3_S3_P1V0S3REG (38)
=P1V0S3_EN (38)

PP1V0_S3
MIN LINE WIDTH=0.4 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=1V
MAKE BASE=TRUE

PP1V0_S3_REG (38)
=PP1V0_S3_USB (32)

Digital Ground

GND
MIN LINE WIDTH=0.6MM
MIN NECK WIDTH=0.2MM
VOLTAGE=0V

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: Power Aliases

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DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 8 OF 110
SHEET: 6 OF 48

PCIe Assignments

23 IN PCIE_T29_R2D_C_P<0>	PCIE_USB_R2D_C_P MAKE_BASE=TRUE	OUT 32 46
23 IN PCIE_T29_R2D_C_N<0>	PCIE_USB_R2D_C_N MAKE_BASE=TRUE	OUT 32 46
23 OUT PCIE_T29_D2R_P<0>	PCIE_USB_D2R_P MAKE_BASE=TRUE	IN 32 46
23 OUT PCIE_T29_D2R_N<0>	PCIE_USB_D2R_N MAKE_BASE=TRUE	IN 32 46
23 IN T29_PCIE_RESET_L<0>	USB_RESET_L MAKE_BASE=TRUE	OUT 32
23 IN PCIE_T29_R2D_C_P<1>	PCIE_ENET_R2D_C_P MAKE_BASE=TRUE	OUT 26 46
23 IN PCIE_T29_R2D_C_N<1>	PCIE_ENET_R2D_C_N MAKE_BASE=TRUE	OUT 26 46
23 OUT PCIE_T29_D2R_P<1>	PCIE_ENET_D2R_P MAKE_BASE=TRUE	IN 26 46
23 OUT PCIE_T29_D2R_N<1>	PCIE_ENET_D2R_N MAKE_BASE=TRUE	IN 26 46
23 IN T29_PCIE_RESET_L<1>	ENET_RESET_L MAKE_BASE=TRUE	OUT 26
23 IN PCIE_T29_R2D_C_P<2>	PCIE_FW_R2D_C_P MAKE_BASE=TRUE	OUT 28 46
23 IN PCIE_T29_R2D_C_N<2>	PCIE_FW_R2D_C_N MAKE_BASE=TRUE	OUT 28 46
23 OUT PCIE_T29_D2R_P<2>	PCIE_FW_D2R_P MAKE_BASE=TRUE	IN 28 46
23 OUT PCIE_T29_D2R_N<2>	PCIE_FW_D2R_N MAKE_BASE=TRUE	IN 28 46
23 IN T29_PCIE_RESET_L<2>	FW_RESET_L MAKE_BASE=TRUE	OUT 28
23 IN PCIE_T29_R2D_C_P<3>	NC_PCIE_T29_R2D_C_P3 MAKE_BASE=TRUE NO_TEST=TRUE	
23 IN PCIE_T29_R2D_C_N<3>	NC_PCIE_T29_R2D_C_N3 MAKE_BASE=TRUE NO_TEST=TRUE	
23 OUT PCIE_T29_D2R_P<3>	NC_PCIE_T29_D2R_P3 MAKE_BASE=TRUE NO_TEST=TRUE	
23 OUT PCIE_T29_D2R_N<3>	NC_PCIE_T29_D2R_N3 MAKE_BASE=TRUE NO_TEST=TRUE	
23 IN T29_PCIE_RESET_L<3>	NC_T29_PCIE_RESET_L3 MAKE_BASE=TRUE NO_TEST=TRUE	

INTERNAL DP PANEL AC COUPLING CAPS

44 7 IN DP_INT_ML_C_P<0>	C900 0.1UF 10% 16V X5R 402		DP_INT_ML_P<0> OUT 21 44 48
44 7 IN DP_INT_ML_C_N<0>	C901 0.1UF 10% 16V X5R 402		DP_INT_ML_N<0> OUT 21 44 48
44 7 IN DP_INT_ML_C_P<1>	C902 0.1UF 10% 16V X5R 402		DP_INT_ML_P<1> OUT 21 44 48
44 7 IN DP_INT_ML_C_N<1>	C903 0.1UF 10% 16V X5R 402		DP_INT_ML_N<1> OUT 21 44 48
44 7 IN DP_INT_ML_C_P<2>	C904 0.1UF 10% 16V X5R 402		DP_INT_ML_P<2> OUT 21 44 48
44 7 IN DP_INT_ML_C_N<2>	C905 0.1UF 10% 16V X5R 402		DP_INT_ML_N<2> OUT 21 44 48
44 7 IN DP_INT_ML_C_P<3>	C906 0.1UF 10% 16V X5R 402		DP_INT_ML_P<3> OUT 21 44 48
44 7 IN DP_INT_ML_C_N<3>	C907 0.1UF 10% 16V X5R 402		DP_INT_ML_N<3> OUT 21 44 48
44 7 IN DP_INT_AUXCH_C_P	C908 0.1UF 10% 16V X5R 402		DP_INT_AUXCH_P OUT 21 44 48
44 7 IN DP_INT_AUXCH_C_N	C909 0.1UF 10% 16V X5R 402		DP_INT_AUXCH_N OUT 21 44 48

Misc Ethernet Aliases

26 OUT ENET_LOW_PWR	TP_ENET_LOW_PWR MAKE_BASE=TRUE

Misc FireWire Aliases

28 IN FW_PME_L	TP_FW_WAKE_L MAKE_BASE=TRUE

T29 NOCONNECTS DUE TO SINGLE PORT AND NO DPOUT

42 7 IN DP_A_PWRDWN		NC_DP_A_PWRDWN MAKE_BASE=TRUE NO_TEST=TRUE
42 34 OUT PM_DPO_EN	R908 4.7K 5% 1/16W MF-LF 402	

INTERNAL DP PANEL SOURCE MUX BYPASS

23 IN DP_T29SRCA_ML_C_P<0>	DP_INT_ML_C_P<0> MAKE_BASE=TRUE	OUT 7 44
23 IN DP_T29SRCA_ML_C_N<0>	DP_INT_ML_C_N<0> MAKE_BASE=TRUE	OUT 7 44
23 IN DP_T29SRCA_ML_C_P<1>	DP_INT_ML_C_P<1> MAKE_BASE=TRUE	OUT 7 44
23 IN DP_T29SRCA_ML_C_N<1>	DP_INT_ML_C_N<1> MAKE_BASE=TRUE	OUT 7 44
23 IN DP_T29SRCA_ML_C_P<2>	DP_INT_ML_C_P<2> MAKE_BASE=TRUE	OUT 7 44
23 IN DP_T29SRCA_ML_C_N<2>	DP_INT_ML_C_N<2> MAKE_BASE=TRUE	OUT 7 44
23 IN DP_T29SRCA_ML_C_P<3>	DP_INT_ML_C_P<3> MAKE_BASE=TRUE	OUT 7 44
23 IN DP_T29SRCA_ML_C_N<3>	DP_INT_ML_C_N<3> MAKE_BASE=TRUE	OUT 7 44
23 BI DP_T29SRCA_AUXCH_C_P	DP_INT_AUXCH_C_P MAKE_BASE=TRUE	BI 7 44
23 BI DP_T29SRCA_AUXCH_C_N	DP_INT_AUXCH_C_N MAKE_BASE=TRUE	BI 7 44
23 OUT DP_T29SRCA_HPD	DP_INT_HPD MAKE_BASE=TRUE	IN 21

MISC T29 ALIAS CONNECTIONS

41 34 IN T29_LSX_R2P MAKE_BASE=TRUE	=T29_LSX_R2P	OUT 34
41 34 OUT T29_LSX_P2R MAKE_BASE=TRUE	=T29_LSX_P2R	IN 34
TP_T29_A_BIAS MAKE_BASE=TRUE	T29_A_BIAS	IN 42
43 6 IN =PP3V3_S4_DPAPWRSW	R909 0 5% 1/16W MF-LF 402	DPAPWRSW_EN MAKE_BASE=TRUE =DPAPWRSW_EN OUT 43
U5000 IS SLAVE MCU - U9330 IS MASTER (SEE REFERENCE DESIGN)	=TCMCU_ADDR	OUT 34

CLOCKS

22 IN PCIE_CLK100M_PCIBR_P	PCIE_CLK100M_USB_P MAKE_BASE=TRUE	OUT 32 46
22 IN PCIE_CLK100M_PCIBR_N	PCIE_CLK100M_USB_N MAKE_BASE=TRUE	OUT 32 46
22 7 OUT PCIBR_CLKREQ_L	PCIE_CLKREQ4 MAKE_BASE=TRUE	
22 IN PCIE_CLK100M_T29S_P	NC_PCIE_CLK100M_SRC6P MAKE_BASE=TRUE NO_TEST=TRUE	
22 IN PCIE_CLK100M_T29S_N	NC_PCIE_CLK100M_SRC6N MAKE_BASE=TRUE NO_TEST=TRUE	
22 OUT T29S_CLKREQ_L	PCIE_CLKREQ6 MAKE_BASE=TRUE	
22 IN PCIE_CLK100M_SLOT_P	NC_PCIE_CLK100M_SRC1P MAKE_BASE=TRUE NO_TEST=TRUE	
22 IN PCIE_CLK100M_SLOT_N	NC_PCIE_CLK100M_SRC1N MAKE_BASE=TRUE NO_TEST=TRUE	
22 OUT PCIESLOT_CLKREQ_L	PCIE_CLKREQ1 MAKE_BASE=TRUE	
22 IN PCIE_CLK100M_SATA_P	NC_PCIE_CLK100M_SRC9P MAKE_BASE=TRUE NO_TEST=TRUE	
22 IN PCIE_CLK100M_SATA_N	NC_PCIE_CLK100M_SRC9N MAKE_BASE=TRUE NO_TEST=TRUE	
22 OUT SATA_CLKREQ_L	PCIE_CLKREQ9 MAKE_BASE=TRUE	
22 IN FW_CLK24P576M	NC_FW_CLK24P576M MAKE_BASE=TRUE NO_TEST=TRUE	
22 IN PS161_CLK27M_R	NC_CLK27M MAKE_BASE=TRUE NO_TEST=TRUE	
22 IN PCI_CLK33M_PCIBR	NC_PCI0_CLK33M MAKE_BASE=TRUE NO_TEST=TRUE	
22 IN PCI_CLK33M_NECUSB	NC_PCI2_CLK33M MAKE_BASE=TRUE NO_TEST=TRUE	

PCIE CLKREQ ENABLING

22 7 IN PCIBR_CLKREQ_L MAKE_BASE=TRUE	R902 0 5% 1/16W MF-LF 402	
22 IN T29_CLKREQ_L MAKE_BASE=TRUE	R903 0 5% 1/16W MF-LF 402	

UNUSED T29S GREENCLK

R990 0 5% 1/16W MF-LF 402	=PPVDDIO_S0_T29S_CLK OUT 22	PPVDDIO_S0_T29S_CLK MAKE_BASE=TRUE
22 IN SYSCLK_CLK25M_T29S	NC_SYSCLK_CLK25M_T29S MAKE_BASE=TRUE NO_TEST=TRUE	

Power-Up Reset Generation

6 =PP3V3_S4_DEVRESET
6 =PP3V3_S0_DEVRESET

Q0910.3 POWERED BY S4 TO ENSURE no glitch when S0 powers-up.

R913 100K 5% 1/10W MF LF 402

S0_RESET_L MAKE_BASE=TRUE — I330 — T29_RESET_L OUT 23

R912 470K 5% 1/10W MF LF 402

R910 100K 5% 1/10W MF LF 402

S0_RESET

Q910 DMB53D0UV SOT-563

DEVRESET_P3V3_RC 100ms delay

C910 1UF 10% 6.3V CERM 402

Q910 DMB53D0UV SOT-563

Wake Sources Power State Isolation

ENSURES THAT DEVICES OFF IN S3 DO NOT DRAG DOWN TBLT_WAKE_L.

26 25 =PP3V3_S3_ENET_PHY_FET

R950 100K 5% 1/10W MF LF 402

Q950 SSM3K15FV SOD VESM HF

26 IN =ENET_WAKE_L — ENET_WAKE_L MAKE_BASE=TRUE — TBLT_WAKE_L MAKE_BASE=TRUE OUT 34 42

35 32 6 =PP3V3_S3_USB

R952 100K 5% 1/10W MF LF 402

Q952 SSM3K15FV SOD VESM HF

32 IN =USB_WAKE_L — USB_WAKE_L MAKE_BASE=TRUE

T29 GPIO TO DETECT ERRANT PASSIVE DP CABLE CONNECTION

24 23 11 7 6 =PP3V3_S0_T29P

R900 10K 5% 1/16W MF LF 402

Q900 SSM3K15FV SOD VESM HF

23 IN T29_GPIO<1> — DP_A_PWRDWN OUT 7 42

UNUSED T29 ROUTER GPIOS

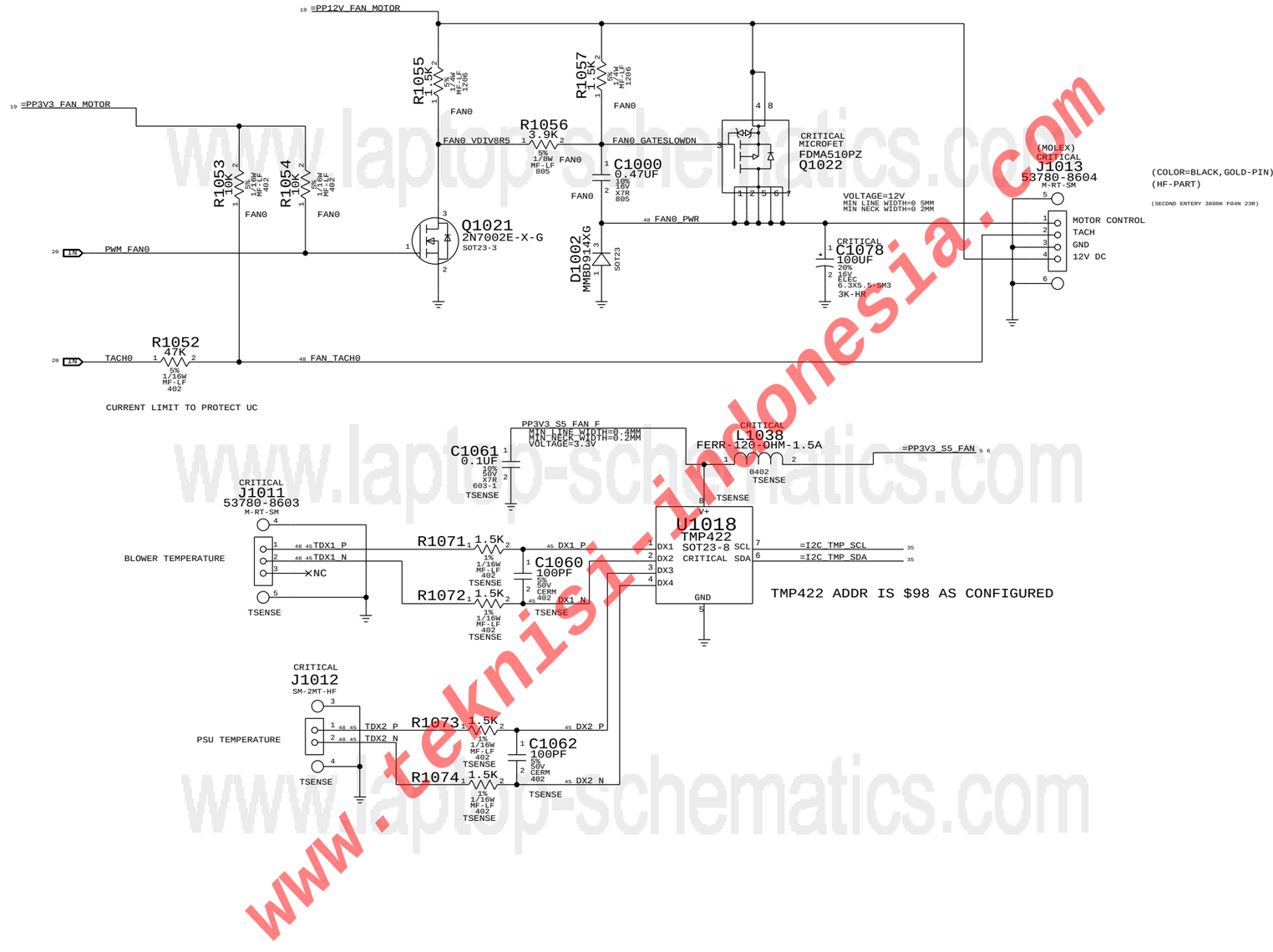
23 BI T29_GPIO<2> — R901 10K 5% 1/10W MF-LF 402 — =PP3V3_S0_T29P 6 7 11 23 24

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 9 OF 110
SHEET 7 OF 48

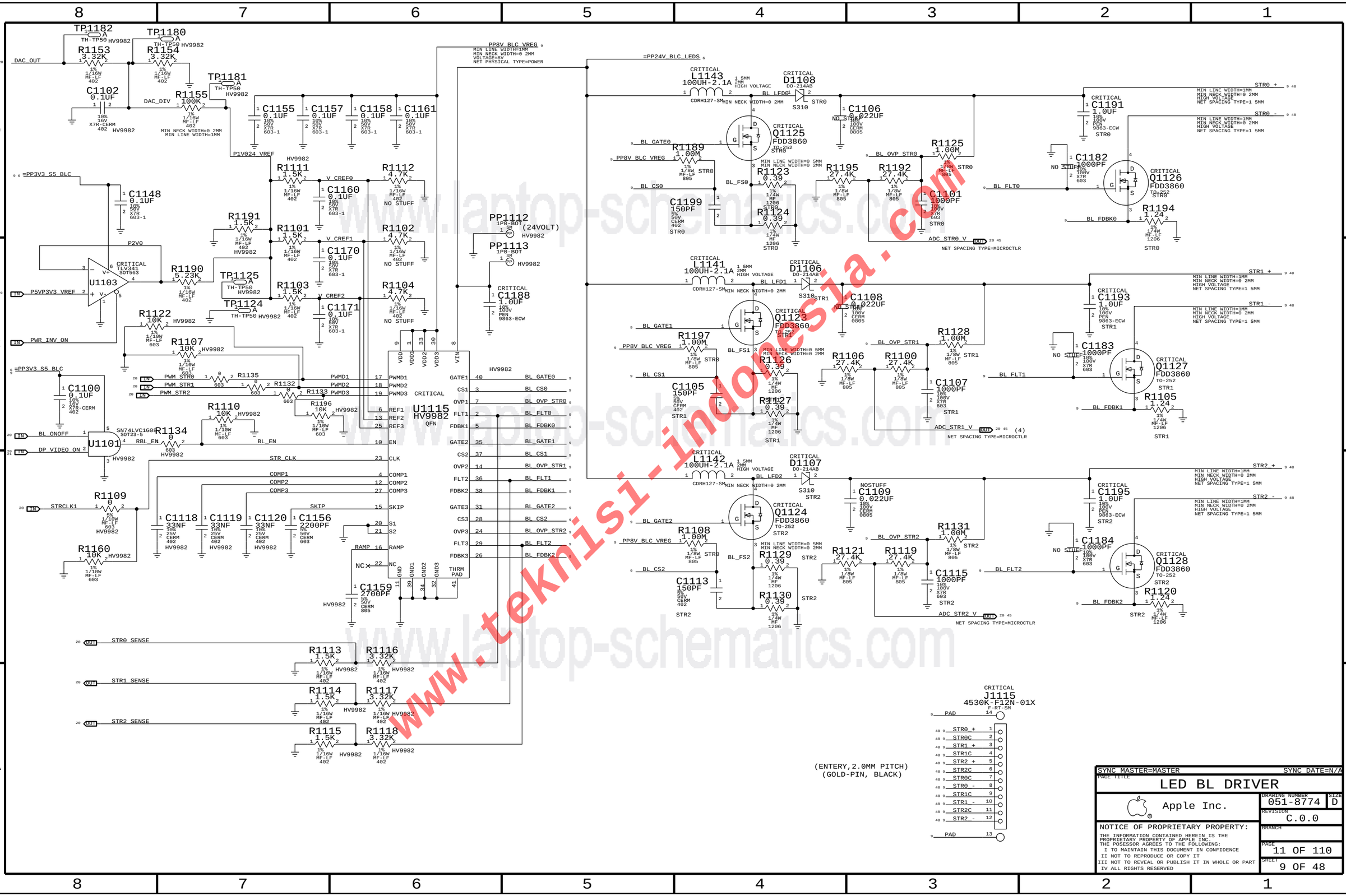


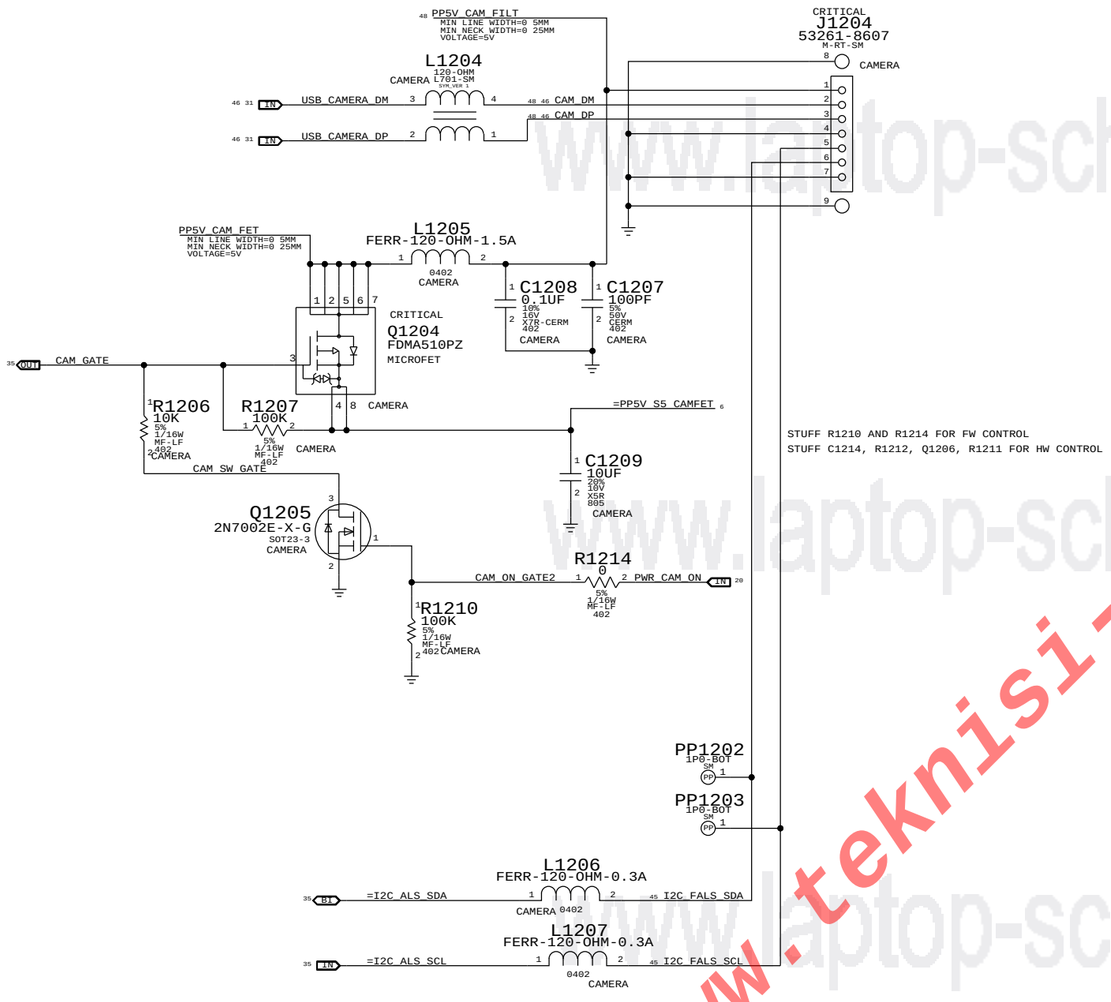
SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
FAN CNTRL & TSENSE

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 10 OF 110
SHEET 8 OF 48





STUFF R1210 AND R1214 FOR FW CONTROL
STUFF C1214, R1212, Q1206, R1211 FOR HW CONTROL

SYNC_MASTER=MASTER SYNC_DATE=N/A

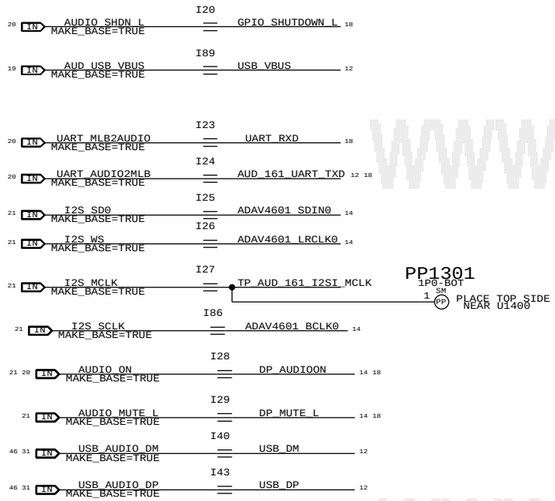
PAGE TITLE: CAMERA/ALS

Apple Inc.

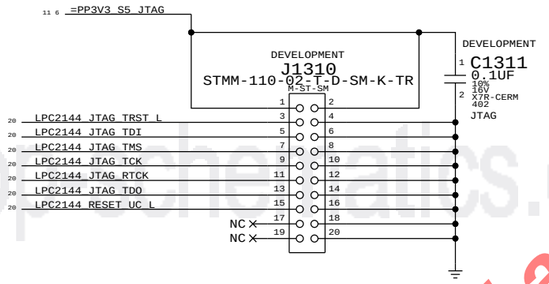
DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 12 OF 110
SHEET: 10 OF 48

T29 JTAG AND DEBUG

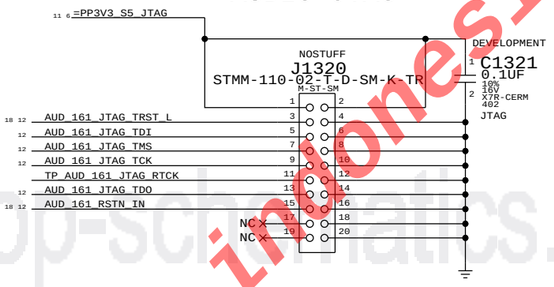
AUDIO ALIASES

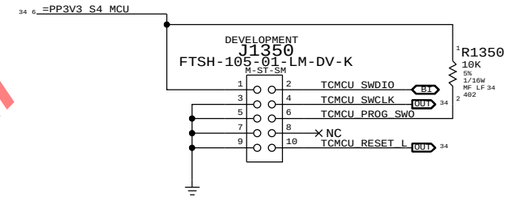


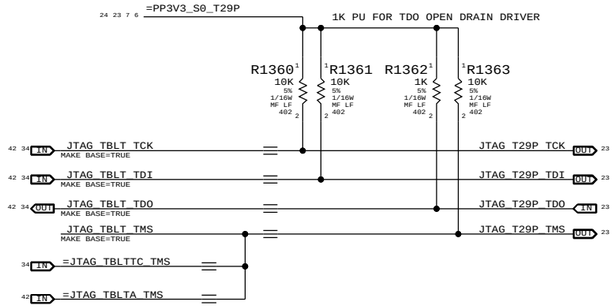
SYSTEM MICRO JTAG



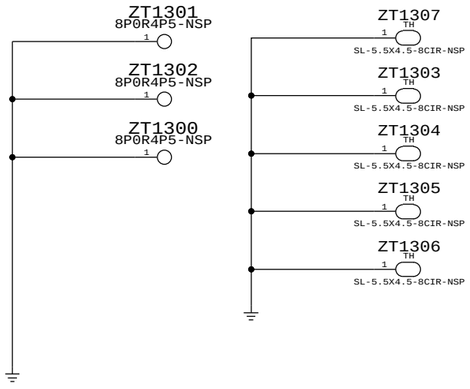
AUDIO JTAG



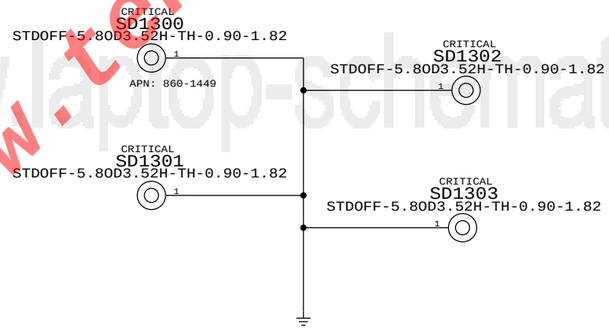




MOUNTING HOLES



J9000 TETHERED CABLE CLAMP STANDOFFS



SYNC MASTER=K59 SYNC DATE=08/22/2010

PAGE TITLE: DEBUG, MISC & JTAG

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 13 OF 110
SHEET: 11 OF 48

USB AUDIO CODEC
APN 353S2320

12.000 MHZ CRYSTAL
APN 197S0264

CRITICAL
Y1400
SN-3.2X2.5MM
12.000MHZ-30PPM-10PF

C1428 22PF 5% 50V CERM 402
C1429 22PF 5% 50V CERM 402

TIE PNX0161_PSU_STOP LOW IF USING INTERNAL 1.8 & 3.3 V SUPPLIES, HIGH IF USING EXTERNAL SUPPLIES

L1400 FERR-220-OHM 0402
L1401 FERR-220-OHM 0402
L1402 FERR-220-OHM 0402
L1405 FERR-1000-OHM 0402
L1406 FERR-1000-OHM 0402
L1407 FERR-1000-OHM 0402
L1408 FERR-1000-OHM 0402

PLACE C1406 NEAR FLASH_VDD_HV PIN
PLACE C1412 & C1413 NEAR XTALL_VDDA18 PIN
PLACE C1414 NEAR XTALH_VDDA18 PIN
PLACE C1436 NEAR MIC_VREFSUP PIN (B4)
PLACE C1437 NEAR ADC_VREF PIN (B1)

U1400 PNX0161 TFBGA
OMIT_TABLE
CRITICAL

R1417 240 5% 1/16W MF-LF 402
R1423 1.5K 1% 1/16W MF-LF 402
R1424 100 5% 1/16W MF-LF 402
R1421 18 1% 1/16W MF 402
R1422 18 1% 1/16W MF 402
R1430 0 5% 1/16W MF-LF 402
R1431 100K 5% 1/16W MF-LF 402

Q1400 NTR1P02L SOT23-3-HF

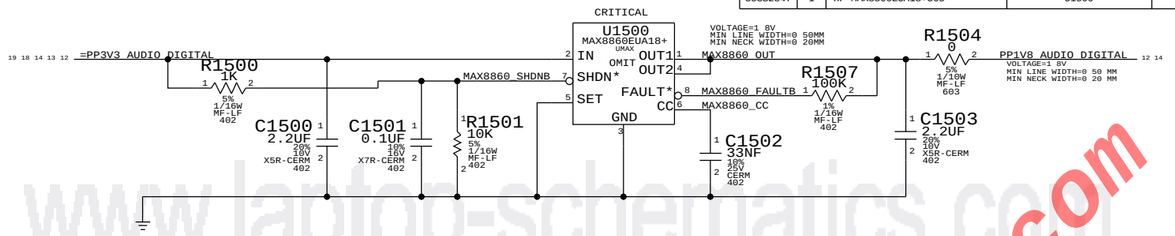
C1432 330PF 5% 50V COG 402
C1433 330PF 5% 50V COG 402

R1425 47K 5% 1/16W MF-LF 402
R1426 47K 5% 1/16W MF-LF 402
R1400 1.5K 1% 1/16W MF-LF 402
R1401 1.5K 1% 1/16W MF-LF 402
R1402 33 5% 1/16W MF-LF 402
R1403 33 5% 1/16W MF-LF 402
R1404 33 5% 1/16W MF-LF 402
R1405 33 5% 1/16W MF-LF 402
R1407 33 5% 1/16W MF-LF 402
R1408 33 5% 1/16W MF-LF 402
R1409 33 5% 1/16W MF-LF 402
R1410 33 5% 1/16W MF-LF 402
R1411 47K 5% 1/16W MF-LF 402
R1412 47K 5% 1/16W MF-LF 402
R1413 47K 5% 1/16W MF-LF 402
R1414 47K 5% 1/16W MF-LF 402
R1415 47K 5% 1/16W MF-LF 402
R1416 47K 5% 1/16W MF-LF 402

PAGE TITLE	PNX0161 CODEC
	Apple Inc.
DRAWING NUMBER	051-8774
SIZE	D
REVISION	C.0.0
BRANCH	
PAGE	14 OF 110
SHEET	12 OF 48

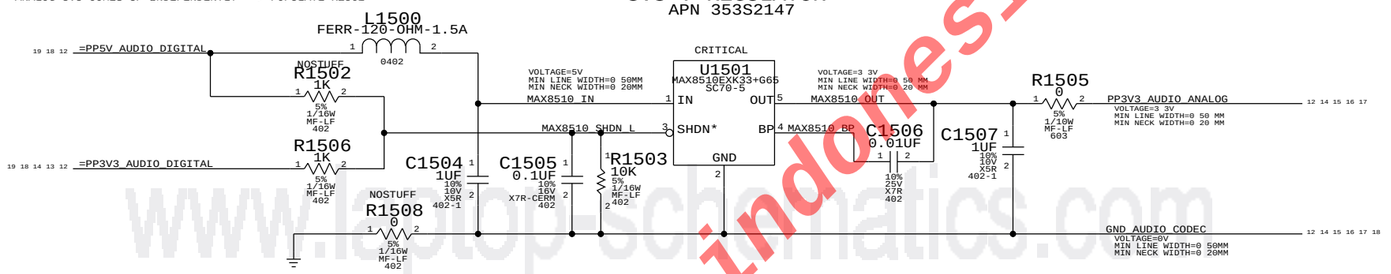
1.8 V REGULATOR
APN 353S2847

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S2847	1	HF MAX8860EUA18+G65	U1500	



6/16 IT'S UNCLEAR IF ANALOG 3.3 V NEEDS TO COME UP WITH DIGITAL 3.3 V,
OR IF IT CAN COME UP INDEPENDENTLY (WITH 5.0 V).
ANALOG 3.3 COMES UP WITH DIGITAL 3.3 --> POPULATE R1506
ANALOG 3.3 COMES UP INDEPENDENTLY --> POPULATE R1502

3.3 V REGULATOR
APN 353S2147



PAGE TITLE
AUDIO DC-DC REGULATORS

Apple Inc.

DRAWING NUMBER 051-8774 | SIZE D
REVISION C.0.0
BRANCH
PAGE 15 OF 110
SHEET 13 OF 48

AUDIO SIGNAL PROCESSOR
APN 337S3285

PLACE C1601 NEAR PIN 4 (ADC POWER SUPPLY)
PLACE C1602 & C1603 NEAR PINS 68 & 71, RESPECTIVELY (DAC POWER SUPPLIES)
PLACE C1604 & C1605 NEAR PIN 59 (HEADPHONE POWER SUPPLY)
PLACE C1606, C1607, & C1608 NEAR PIN 53 (PLL POWER SUPPLY)

PLACE R1604 AS CLOSE AS POSSIBLE TO U1601 PIN 33

GND CONNECTIONS WERE ADDED TO ADDRESS EMI CONCERNS ON K59

PAGE TITLE	SIGMA DSP
	Apple Inc.
DRAWING NUMBER	051-8774
SIZE	D
REVISION	C.0.0
BRANCH	
PAGE	16 OF 110
SHEET	14 OF 48

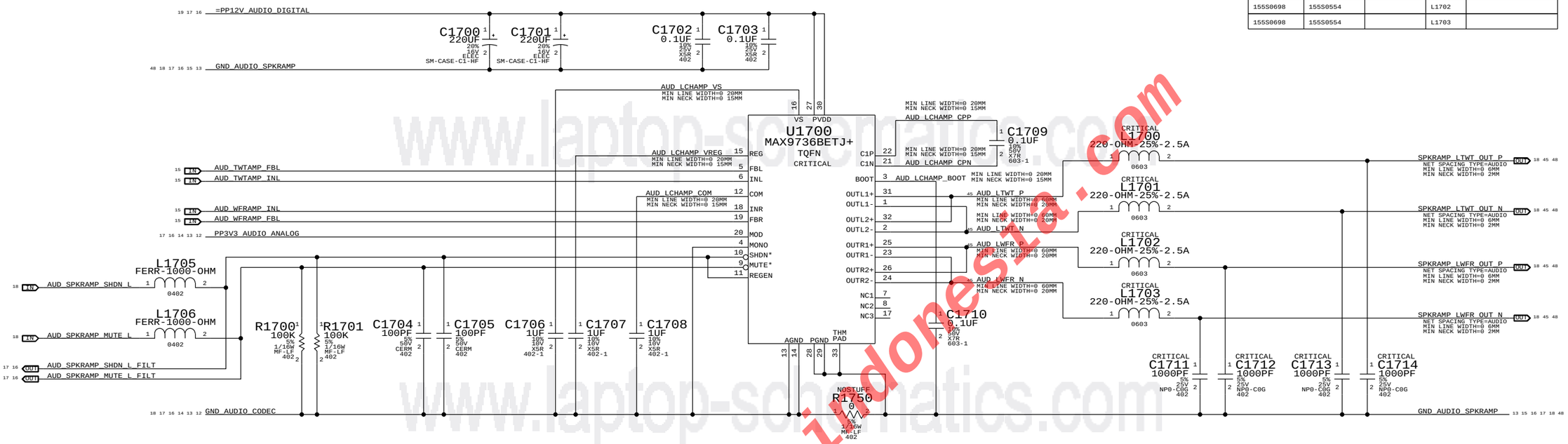
LEFT SPEAKER AMP

APN 353S2042

GAIN = 7.36 V/V (+17.33 DB)

FC = ~774 HZ (TWEETER), ~12 HZ (WOOFER)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1700	
155S0698	155S0554		L1701	
155S0698	155S0554		L1702	
155S0698	155S0554		L1703	

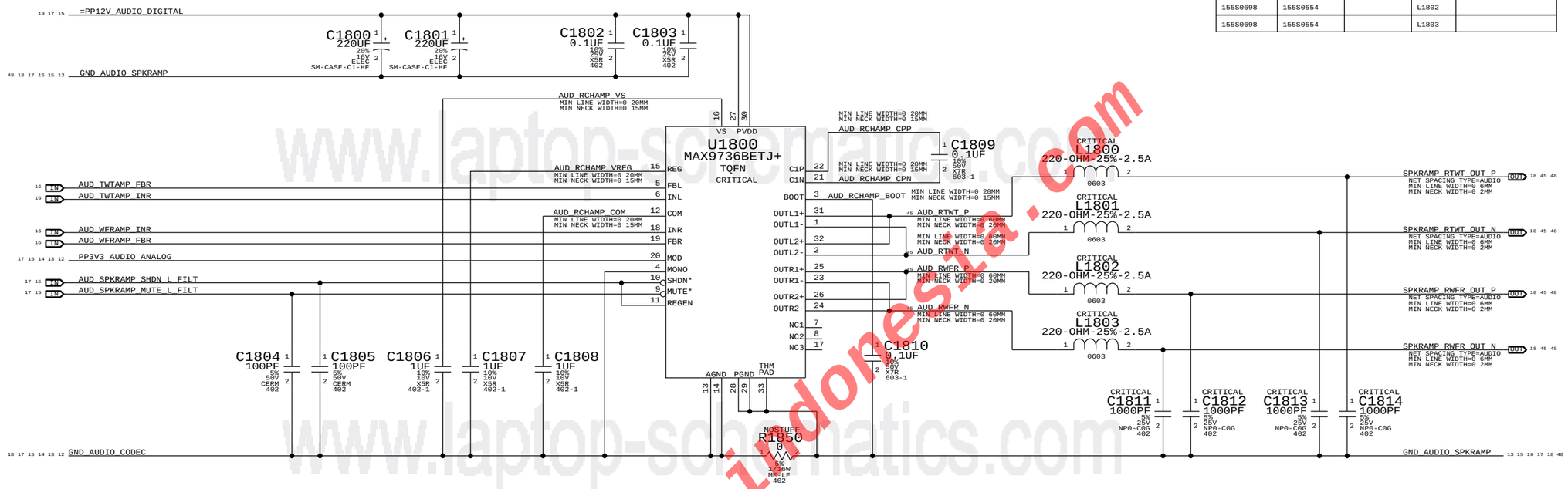


PAGE TITLE	LEFT SPEAKER AMP
	Apple Inc.
DRAWING NUMBER	051-8774
SIZE	D
REVISION	C.0.0
BRANCH	
PAGE	17 OF 110
SHEET	15 OF 48

RIGHT SPEAKER AMP

APN 353S2042
GAIN = 7.36 V/V (+17.33 DB)
FC = ~774 HZ (TWEETER), ~12 HZ (WOOFER)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1800	
155S0698	155S0554		L1801	
155S0698	155S0554		L1802	
155S0698	155S0554		L1803	



PAGE TITLE	RIGHT SPEAKER AMP
	Apple Inc.
DRAWING NUMBER	051-8774
SIZE	D
REVISION	C.0.0
BRANCH	
PAGE	18 OF 110
SHEET	16 OF 48

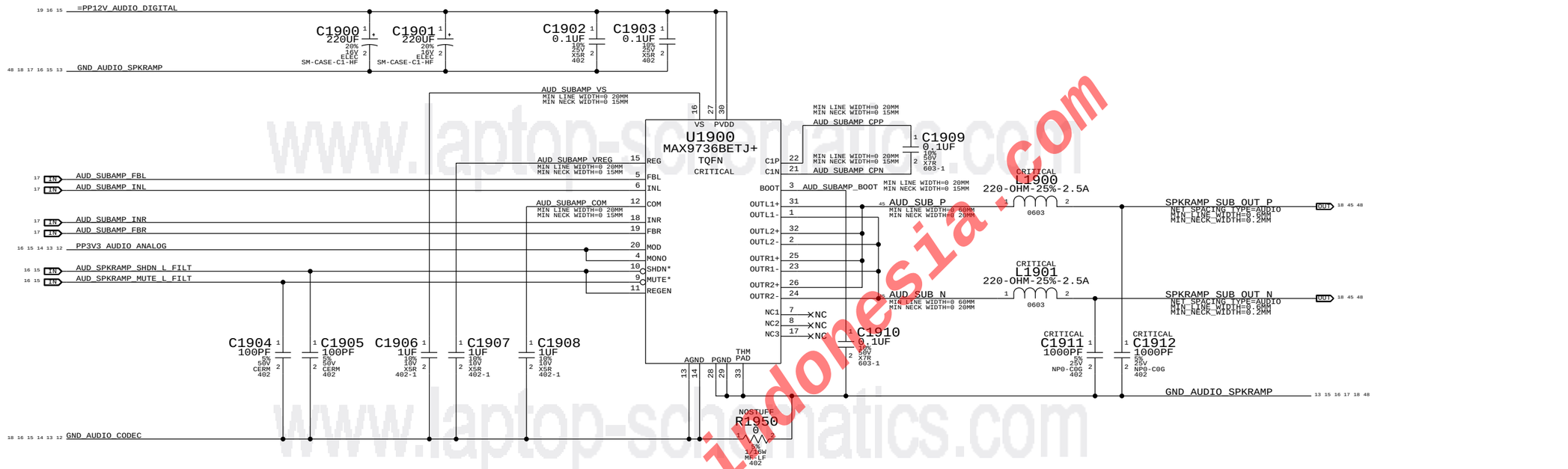
SUBWOOFER SPEAKER AMP

APN 353S2042

GAIN = 7.36 V/V (+17.33 DB)

FC = ~12 HZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1900	
155S0698	155S0554		L1901	



PAGE TITLE: SUBWOOFER SPEAKER AMP

Apple Inc.

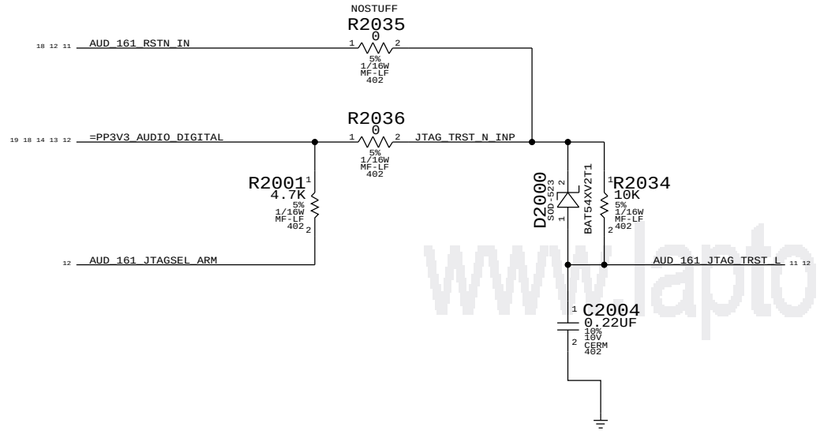
DRAWING NUMBER: 051-8774 SIZE: D

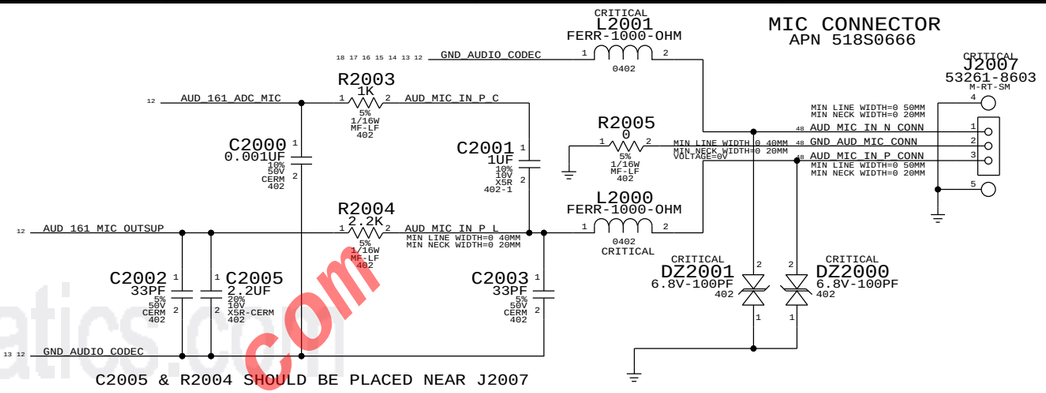
REVISION: C.0.0

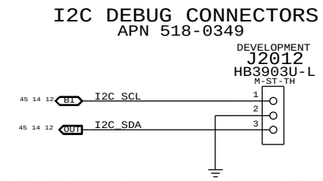
BRANCH:

PAGE: 19 OF 110

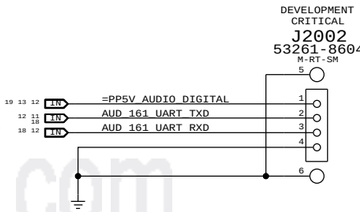
SHEET: 17 OF 48

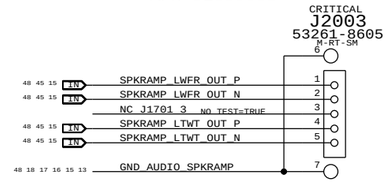


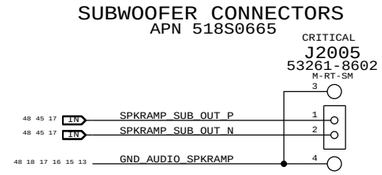


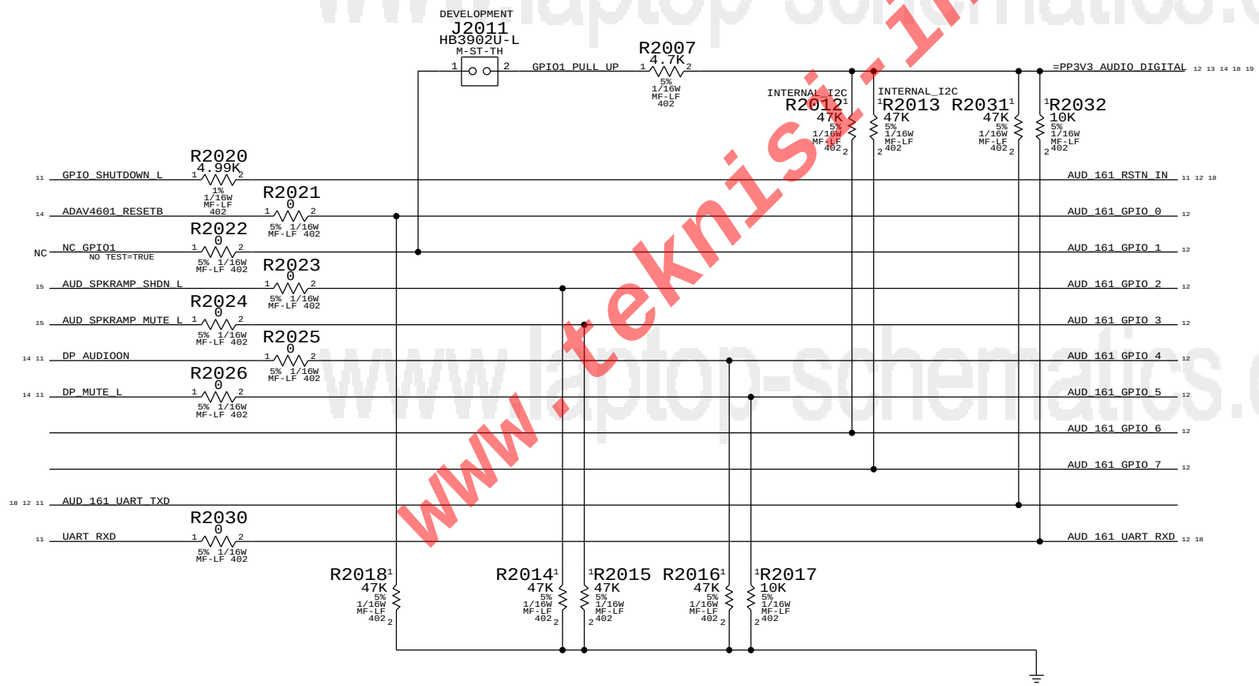


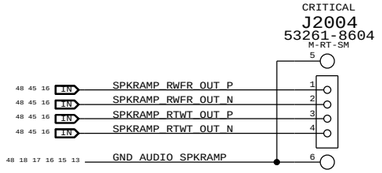
FIXME!!! 3-PIN VERSION NOT RELEASED IN AGILE?
ROW, ROW, ROW YOUR BOAT, GENTLY DOWN THE STREAM.
HA HA, FOOLED YOU, I'M A SUBMARINE.











PAGE TITLE
AUDIO CONNECTORS

Apple Inc.

DRAWING NUMBER 051-8774 | SIZE D
REVISION C.0.0
BRANCH
PAGE 20 OF 110
SHEET 18 OF 48

FAN SWITCH

=PP12V_S5_LCDFET
C2317 0.47UF 10% 16V X7R 805
R2353 100K 5% 1/16W MF-LF 402
GATE_12VLCD
NOSTUFF C2320 0.047UF 10% 25V X5R 0402
CRITICAL Q2318 FDMA510PZ MICROFET SW1_VLCD
PP2314 1P0-BOT SM
PP2315 1P0-BOT SM
SW1_VLCD
R2300 10K 1% 1/10W MF-LF 603
PP12V_LCD_FET MIN_LINE_WIDTH=1.0MM MIN_NECK_WIDTH=0.25MM VOLTAGE=12V MAKE_BASE=TRUE
=PP12V_LCD_PANEL 21
R2315 68K 5% 1/10W MF-LF 603
PWR_PANEL_ON_DIV
PWR_PANEL_ON_INV
SW1_VLCD
PWR_PANEL_ON 20
R2327 10K 5% 1/16W MF-LF 402 SW1_VLCD
Q2304 MMBT3904G SOT23 SW1_VLCD
R2301 10K 5% 1/16W MF-LF 402 SW1_VLCD

P4_PWR_INV_DIV
P4_PWR_INV
R2382 10K 5% 1/16W MF-LF 402 AUDIO_VB
Q2354 2N3906 SOT23-HF AUDIO_VB
AUD_USB_VBUS 11
R2384 100K 5% 1/16W MF-LF 402 AUDIO_VB
R2383 100K 5% 1/16W MF-LF 402 AUDIO_VB
PP5V_AUDIO_FET 19
C2380 0.1UF 10% 50V X7R 603-1 AUDIO_VB
R2380 10K 5% 1/16W MF-LF 402 AUDIO_VB
P4_PWR 31
P4_PWR_DIV
Q2355 MMBT3904G SOT23 AUDIO_VB
R2381 10K 5% 1/16W MF-LF 402 AUDIO_VB

PP2319 1P0-BOT SM SWI_FAN3
PP2318 1P0-BOT SM SWI_FAN3
PP3V3_FAN_BUF MIN_LINE_WIDTH=1.0MM MIN_NECK_WIDTH=0.25MM VOLTAGE=3.3V MAKE_BASE=TRUE
PWR_FAN_ON_INV2_DIV
PWR_FAN_ON_INV2
R2330 10K 5% 1/16W MF-LF 402 SWI_FAN3
Q2307 2N3906 SOT23-HF SWI_FAN3
=PP3V3_FAN_MOTOR 8
R2303 100K 5% 1/16W MF-LF 402 SWI_FAN3
=PP3V3_S5_FANBUF 6
C2319 0.1UF 10% 50V X7R 603-1 SWI_FAN3
PP2316 1P0-BOT SM SWI_FAN12
PP2317 1P0-BOT SM SWI_FAN12
PP12V_FAN_FET MIN_LINE_WIDTH=1.0MM MIN_NECK_WIDTH=0.25MM VOLTAGE=12V MAKE_BASE=TRUE
=PP12V_FAN_MOTOR 8
R2320 10K 5% 1/16W MF-LF 402 SWI_FAN3
PWR_FAN_ON_DIV2
Q2306 MMBT3904G SOT23 SWI_FAN3
R2321 10K 5% 1/16W MF-LF 402 SWI_FAN3

=PP12V_S5_FANFET 6
C2318 0.1UF 10% 50V X7R 603-1 SWI_FAN12
R2302 100K 5% 1/16W MF-LF 402
GATE_12VFAN
CRITICAL Q2300 FDMA510PZ MICROFET SWI_FAN12
R2319 100K 5% 1/10W MF-LF 603 SWI_FAN12
PWR_FAN_ON_INV
PWR_FAN_ON 20
R2316 10K 5% 1/16W MF-LF 402 SWI_FAN12
PWR_FAN_ON_DIV
Q2305 MMBT3904G SOT23 SWI_FAN12
C2316 0.018UF 10% 16V X7R 402 SWI_FAN12
R2317 10K 5% 1/16W MF-LF 402 SWI_FAN12

PP2322 1P0-BOT SM
PP2323 1P0-BOT SM SWI_VAUD
SWI_VAUD
PP12V_AUDIO_FET MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=12V MAKE_BASE=TRUE
=PP12V_AUDIO_DIGITAL 15 16 17
SWI_VAUD MIN_NECK_WIDTH=0.2MM MIN_LANE_WIDTH=0.6MM
RT2306 0 5% 1/4W MF-LF 1206
VCC12V_AUD_S
CRITICAL Q2319 FDS4465_G SOI-HF SWI_VAUD
R2379 10K 1% 1/10W MF-LF 603
=PP12V_S5_AUDIOFET 6
C2324 0.47UF 10% 16V X7R 805 SWI_VAUD
R2332 68K 5% 1/10W MF-LF 603
GATE_12VAUDIO
VDIV_GATE
R2378 220K 5% 1/10W MF-LF 603 SWI_VAUD
R2331 499K 1% 1/10W MF-LF 603
PWR_AUDIO12V_ON_INV
R2328 10K 5% 1/16W MF-LF 402
PWR_AUDIO12V_ON 20
PWR_AUDIO12V_ON_DIV
Q2310 MMBT3904G SOT23 SWI_VAUD
R2329 10K 5% 1/16W MF-LF 402 SWI_VAUD

=PP5V_S5_AUDIOFET 6
SWI_VAUD5 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RT2350 0 5% 1/4W MF-LF 1206
VCC5V_AUD_S
CRITICAL Q2350 SI3443CDV TSOP-6
PP5V_AUDIO_FET MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V MAKE_BASE=TRUE
=PP5V_AUDIO_DIGITAL 12 13 18
C2370 0.1UF 10% 50V X7R 603-1 SWI_VAUD5
R2370 100K 5% 1/16W MF-LF 402
GATE_5VAUDIO
SWI_VAUD5
R2385 10K 1% 1/10W MF-LF 603
R2371 10K 1% 1/10W MF-LF 603
PWR_AUDIO5V_ON_INV
R2373 10K 5% 1/16W MF-LF 402
PWR_AUDIO5V_ON 20 19
PWR_AUDIO5V_ON_DIV
Q2351 MMBT3904G SOT23 SWI_VAUD5
R2372 10K 5% 1/16W MF-LF 402 SWI_VAUD5

=PP3V3_S5_AUDIOFET 6
SWI_VAUD3 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
RT2351 0 5% 1/4W MF-LF 1206
VCC3V3_AUD_S
CRITICAL Q2352 SI3443CDV TSOP-6
PP3V3_AUDIO_FET MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=3.3V MAKE_BASE=TRUE
=PP3V3_AUDIO_DIGITAL 12 13 14 18
C2371 0.1UF 10% 50V X7R 603-1 SWI_VAUD3
R2374 100K 5% 1/16W MF-LF 402
GATE_3VAUDIO
SWI_VAUD3
R2375 10K 1% 1/10W MF-LF 603
R2368 10K 5% 1/16W MF-LF 402
PWR_AUDIO5V_ON 20 19
PWR5V_AUDIO_FET_DLY_INV
NOSTUFF R2376 10K 5% 1/16W MF-LF 402
PWR_AUDIO3V_ON 20
PWR5V_AUDIO_FET_DLY
Q2353 MMBT3904G SOT23 SWI_VAUD3
R2377 10K 5% 1/16W MF-LF 402 SWI_VAUD3
NOSTUFF C2372 0.1UF 10% 50V X7R 603-1 SWI_VAUD3

SYNC_MASTER=MASTER SYNC_DATE=N/A
PAGE TITLE: POWER SW CONTROL
Apple Inc.
DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 23 OF 110
SHEET 19 OF 48

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
311S0394	1	SINGLE NAND GATE SOT553-5	U2608	CRITICAL	

NOTE NOR GATE FOR OLD SYSTEM UC SLEEP NAND GATE FOR DEEP SYSTEM UC SLEEP SLEEP
WARNING DEV CONNECTOR WAKE WILL NO LONGER WORK WITH THIS CONFIGURATION!!!

NOTE DON'T PULLDOWN P0 31 OR JTAG GETS DISABLED!!

SHORT PINS 2 & 3 FOR JTAG BOOT MODE

SYNC MASTER=K59 SYNC DATE=08/22/2010

PAGE TITLE
LPC2144 & PERIPHERALS

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DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 26 OF 110
SHEET 20 OF 48

R2754 10K 5% 1/16W MF-LF 402 — SWVIDEO_ON
R2755 100K 5% 1/16W MF-LF 402 — DP_VIDEO_ON
R2756 10K 5% 1/16W MF-LF 402 — SWVSYNC
R2757 100K 5% 1/16W MF-LF 402 — RVSYNC
R2759 10K 5% 1/16W MF-LF 402 — SWAUDIO_ON
R2763 10K 5% 1/16W MF-LF 402 — I2S_SWSCLK
R2762 10K 5% 1/16W MF-LF 402 — I2S_SWMCLK

R2769 10K 5% 1/16W MF-LF 402 — I2S_SWWS
R2771 10K 5% 1/16W MF-LF 402 — I2S_SWSD0
R2776 10K 5% 1/16W MF-LF 402 — SWAUDIO_MUTE_L

=PP3V3_S5_TCON

R2746 0 5% 1/10W MF-LF 402 NOSTUFF — PP3V3_BUF (MIN LINE WIDTH=0 4MM, MIN NECK WIDTH=0 2MM, VOLTAGE=3 3V)
R2747 0 5% 1/16W MF-LF 402 — PP3V3_DPL_TCON
C2701 0.1UF 10% 16V X7R-CERM 402
R2777 100K 5% 1/16W MF-LF 402
R2775 100K 5% 1/16W MF-LF 402

U2702 74LVC1G125DBVG4 SOT23-5
DP_RX_INT_L → SWDP_RX_INT_L
PP2705 1P0-BOT SM

U2701 TSSOP SN74LVC8T245PW
OE* GND DIR VCCA VCCB
A1 RVSYNC
A2 RI2S_SD0
A3 DP_VIDEO_ON
A4 RI2S_WS
A5 RI2S_SCLK
A6 AUDIO_MUTE_L
A7 AUDIO_ON
A8 RI2S_MCLK
B1 SWVSYNC
B2 SWVIDEO_ON
B3 I2S_SWSD0
B4 I2S_SWWS
B5 I2S_SWSCLK
B6 SWAUDIO_MUTE_L
B7 SWAUDIO_ON
B8 I2S_SWMCLK

I2S_MCLK — R2745 22 5% 1/10W MF-LF 402 K29TC
I2S_SCLK — R2741 22 5% 1/16W MF-LF 402
I2S_WS — R2742 22 5% 1/16W MF-LF 402
I2S_SD0 — R2743 22 5% 1/16W MF-LF 402
VSYNC — R2709 22 5% 1/16W MF-LF 402 K29TC

=PP3V3_S5_TCON — C2772 0.1UF 10% 16V X7R-CERM 402
=PP3V3_S5_TCON — C2776 0.1UF 10% 16V X7R-CERM 402
PP3V3_DPL_TCON

PP2702 1P0-BOT SM — DP_PWR_UP_L
=PP3V3_S5_TCON — R2744 10K 5% 1/16W MF-LF 402

CRITICAL Q2718 SI3443CDV TSOP-6
PP2701 1P0-BOT SM — PP3V3_DPL_TCON (MIN LINE WIDTH=1 0MM, MIN NECK WIDTH=0 2MM, VOLTAGE=3 3V)
R2738 100K 5% 1/16W MF-LF 402
R2739 100K 5% 1/16W MF-LF 402 NO STUFF
R2740 0 5% 1/16W MF-LF 402 — DPL_GATE

Q2710 2N7002E-X-G SOT23-3 — DP_PWR_UP_GATE
R2724 5.1M 5% 1/16W MF-LF 402 K29TC
Q2712 2N7002E-X-G SOT23-3
R2725 5.1M 5% 1/16W MF-LF 402 K29TC
DPRESET
PP2703 1P0-BOT SM
PP2704 1P0-BOT SM

=PP3V3_S5_TCON — C2775 0.1UF 10% 16V X7R-CERM 402

I2C_TCON_ENAB — R2764 10K 5% 1/16W MF-LF 402 — I2C_TCON_ENAB_R
J2710 HB3902U-L M-ST-TH — DEVELOPMENT

R2780 4.7K 5% 1/16W MF-LF 402
R2781 4.7K 5% 1/16W MF-LF 402
U2704 TS5A23166 US8 — V+ IN1 IN2 COM1 COM2 NO1 NO2 GND — CRITICAL — CAMERA

I2C_LPCREM_SCL
I2C_LPCREM_SDA
J2713 HB3902U-L M-ST-TH — DEVELOPMENT

SDA_SWREM
SCL_SWREM
=I2C_DP628_SDA
=I2C_DP628_SCL
J2712 HB3902U-L M-ST-TH — DEVELOPMENT
J2711 HB3902U-L M-ST-TH — DEVELOPMENT

L2712 FERR-120-OHM-0.3A 0402 — DDC_SDA_FC
L2713 FERR-120-OHM-0.3A 0402 — DDC_SCL_FC
L2715 FERR-120-OHM-0.3A 0402 — SDA_FC
L2716 FERR-120-OHM-0.3A 0402 — SCL_FC

=PP3V3_S0_TCON
R2722 100K 5% 1/16W MF-LF 402 — DP_INT_AUXCH_N
R2723 100K 5% 1/16W MF-LF 402 — DP_INT_AUXCH_P

=PP12V_LCD_PANEL
CRITICAL L2740 FERR-120-OHM-3A 0603
CRITICAL L2741 FERR-120-OHM-3A 0603
PP12V_PANEL_FC (MIN LINE WIDTH=1 0MM, MIN NECK WIDTH=0 2MM, VOLTAGE=12V)

CRITICAL J2726 53780-8606 M-RT-SM

NOSTUFF L2746 FERR-120-OHM-0.3A 0402 — NC_I2S_MCLK_FC
L2703 FERR-120-OHM-0.3A 0402 — INT_FC_L
L2705 FERR-120-OHM-0.3A 0402 — AUDIO_ON_FC
L2706 FERR-120-OHM-0.3A 0402 — AUDIO_MUTE_FC_L
L2708 FERR-120-OHM-0.3A 0402 — I2S_SCLK_FC
L2709 FERR-120-OHM-0.3A 0402 — I2S_WS_FC
L2710 FERR-120-OHM-0.3A 0402 — I2S_SD0_FC
L2737 FERR-120-OHM-0.3A 0402 — VIDEO_ON_FC
L2739 FERR-120-OHM-0.3A 0402 — VSYNC_FC
L2702 FERR-120-OHM-0.3A 0402 — DP_PWR_UP_FC

NC_DP_SPDIF (NO TEST)
NC_DP_OPTION1 (NO TEST)
DP_INT_HPD_FC
DP_INT_AUXCH_N
DP_INT_AUXCH_P
DP_INT_ML_P<0>
DP_INT_ML_N<0>
DP_INT_ML_P<1>
DP_INT_ML_N<1>
DP_INT_ML_P<2>
DP_INT_ML_N<2>
DP_INT_ML_P<3>
DP_INT_ML_N<3>
NC_DP_OPTION2 (NO TEST)

COMBINED IN SERIES WITH 47 OHM ON PANEL LIMITS CURRENT TO 20MA
DP_INT_HPD — R2720 120 5% 1/16W MF-LF 402 K29TC

CRITICAL J2725 20474-040E-11 F-RT-SM K29TC

SYNC_MASTER=K59 SYNC_DATE=08/22/2010

PAGE TITLE: DP FC & INTERFACE

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 27 OF 110
SHEET: 21 OF 48

PCI_GEN_SEL	SRC_OUTPUTS
0	Gen 1
1	Gen 2

PCI_SEL	PIN 65
0	24.576MHz
1	33MHz

GCLK_SEL	PIN 5	PIN 6
0	DOT_96+	DOT_96-
1	27M	27M w/SS

FS_C	FS_B	FS_A	CPU MHz
0	0	0	266.6
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	X	X	RSVD

=PP3V3_S0_CK505

L2860
FERR-120-OHM-1.5A
0402

PP3V3_S0_CK505_VDD
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

BYPASS Properties:
U2850 50 53 5 mm
U2850 60 63 5 mm
U2850 67 66 3 mm
U2850 1 3 4 mm
U2850 54 56 4 mm
U2850 4 7 5 mm

C2860 10UF 20% 6.3V X5R 603
C2861 C2862 C2863 C2854 C2855 C2856 0.1UF 10% 16V X5R 402

U2850 11 16 8 mm
U2850 29 32 6 mm
U2850 37 32 8 mm
U2850 44 47 5 mm
=PP1V05_S0_CK505

C2870 C2871 C2872 C2873 0.1UF 10% 16V X5R 402

R2880 R2882 R2884 R2886 R2888 R2890 10K 5% 1/16W MF LF 402
R2881 R2883 R2885 R2887 R2889 10K 5% 1/16W MF LF 402

VDD_CORE VDD_PCI VDD_24 VDD_48 VDD_REF VDD_27 VDD_SRC VDD_CPU

One 0.1uF per power pin (place at pin).
One 10uF cap per filtered rail.

CK505_PWRGD
PCIESLOT_CLKREQ_L
T29_CLKREQ_L
PCIBR_CLKREQ_L
ENET_CLKREQ_L
T29S_CLKREQ_L
FW_CLKREQ_L
SATA_CLKREQ_L
CK505_PCI_STOP_L

U2850
SLG8SP568
QFN
CRITICAL

CKPWRGD/PWRDWN*
CPU_STOP*
CLKREQ_1*
CLKREQ_3*
CLKREQ_4*
CLKREQ_5*
CLKREQ_6*
CLKREQ_8*
CLKREQ_9*
PCI_STOP*
PCIF_0/ITP_EN
PCI_0/PCIE_GEN_SEL (IPD)
PCI_1/PCI_SEL
PCI_2/GCLK_SEL
PCI_3/24.576M/FS_B
48M/FS_A
REF/FS_C
SCL
SDA
XTAL_IN
XTAL_OUT
THRM_PAD

CPU_0 CPU_0* CPU_1 CPU_1* CPU_2_ITP/SRC_10 CPU_2_ITP*/SRC_10* — NC

CPU CLKs Unused

Frequency strapped to 133MHz for lowest lowest power. CPU_STOP* must be enabled via I2C to stop CPU_x outputs.

SRC_0 SRC_0* — NC

Unused 100MHz (no CLKREQ#)

SRC_1 SRC_1* — PCIE_CLK100M_SLOT_P/N

PCIe x4 Slot 100MHz

SRC_2 SRC_2* — NC

Unused 100MHz (no CLKREQ#)

SRC_3 SRC_3* — PCIE_CLK100M_T29_P/N

T29 Primary 100MHz

SRC_4 SRC_4* — PCIE_CLK100M_PCIBR_P/N

PCI Bridge 100MHz

SRC_5 SRC_5* — PCIE_CLK100M_ENET_P/N

Caesar-IV PCIe 100MHz

SRC_6 SRC_6* — PCIE_CLK100M_T29S_P/N

T29 Secondary 100MHz

SRC_7 SRC_7* — NC

Unused 100MHz (no CLKREQ#)

SRC_8 SRC_8* — PCIE_CLK100M_FW_P/N

FireWire PCIe 100MHz

SRC_9 SRC_9* — PCIE_CLK100M_SATA_P/N

SATA 100MHz

DOT_96/27M — PS161_CLK27M_R
DOT_96*/27M_SS — NC

PS161 27MHz Non-Spread
Unused 27MHz Spread

VSS_CORE VSS_PCI VSS_24 VSS_48 VSS_REF VSS_27 VSS_SRC VSS_CPU

PCI CLK33M PCIBR — R2895 33 — PCI CLK33M PCIBR R
PCI CLK33M NECUSB — R2896 33
FW CLK24P576M — R2897 33
5% 1/16W MF LF 402

CK505_PCIE_GEN2_SEL
CK505_24P576M_L
PCI_CLK33M_NECUSB_R
CK505_CLK24P576M_FSB

R2891 R2893 10K 5% 1/16W MF LF 402
R2892 R2894 10K 5% 1/16W MF LF 402

=I2C_CK505_SCL
=I2C_CK505_SDA

CK505_CLK14M_XTAL_IN
CK505_CLK14M_XTAL_OUT

CRITICAL
Y2850
14.31818
5X3 2 SM

C2850 C2851 18PF 5% 50V CERM 402

NEED TO CHECK CAP VALUE

System 25MHz Clock Generator

GreenClk 25MHz Power
Ethernet XTAL Power
T29S XTAL Power
T29P XTAL Power

=PP3V3_ENET_SYSCLK
=PPVDDIO_ENET_CLK
=PPVDDIO_S0_T29S_CLK
=PPVDDIO_S0_T29P_CLK

C2824 C2822 C2820 C2802 0.1UF 20% 10V CERM 402

U2800
SLG3NB146V
TDFN
CRITICAL

VDD VDDIO_A VDDIO_B VDDIO_C GND THRM PAD

C2805 12PF
C2806 12PF
5% 50V CERM 402

SYSCLK_CLK25M_X2
SYSCLK_CLK25M_X1
CRITICAL
Y2805
25.000MHZ-12PF-20PPM
SM 3 2X2 5MM
NC
NC

R2805 0 5% 1/16W MF LF 402
SYSCLK_CLK25M_X2_R
NO STUFF
R2806 1M 5% 1/16W MF LF 402

XOUT
XIN

25MHZ_A — SYSCLK_CLK25M_T29S
25MHZ_B — SYSCLK_CLK25M_ENET
25MHZ_C — SYSCLK_CLK25M_T29

NOTE: 30 PPM crystal required

SYNC_MASTER=T29_D
SYNC_DATE=03/17/2013
PAGE TITLE
T29 Clocking

Apple Inc.

DRAWING NUMBER 051-8774
SIZE D
REVISION C.0.0
BRANCH
PAGE 28 OF 110
SHEET 22 OF 48

CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_T29_D2R_P<0> V19 PER_0_P
PCIE_T29_D2R_N<0> T19 PER_0_N
PCIE_T29_D2R_P<1> P19 PER_1_P
PCIE_T29_D2R_N<1> M19 PER_1_N
PCIE_T29_D2R_P<2> K19 PER_2_P
PCIE_T29_D2R_N<2> H19 PER_2_N
PCIE_T29_D2R_P<3> F19 PER_3_P
PCIE_T29_D2R_N<3> D19 PER_3_N

TRANSMIT

PET_0_P V21 PCIE_T29_R2D_C_P<0>
PET_0_N T21 PCIE_T29_R2D_C_N<0>
PET_1_P P21 PCIE_T29_R2D_C_P<1>
PET_1_N M21 PCIE_T29_R2D_C_N<1>
PET_2_P K21 PCIE_T29_R2D_C_P<2>
PET_2_N H21 PCIE_T29_R2D_C_N<2>
PET_3_P F21 PCIE_T29_R2D_C_P<3>
PET_3_N D21 PCIE_T29_R2D_C_N<3>

TP_T29_MONDC0 — R3610 0 NO STUFF — T29_MONDC0 B21 MONDC0
DEBUG For monitoring current/voltage
TP_T29_MONDC1 — R3611 0 NO STUFF — T29_MONDC1 A20 MONDC1
TP_T29_MONOBSP — C3615 0.1uF — T29_MONOBSP K17 MONOBSP
DEBUG For monitoring clock
TP_T29_MONOBSN — C3616 0.1uF — T29_MONOBSN M17 MONOBSN

=PP3V3_S0_T29P
R3651 10K 5% 1/16W MF LF 402
WAKE* F1 T29_PCIE_WAKE_L
U3600 not powered in sleep, WAKE# input unusable.
PERST* E6 T29_RESET_L
RSENSE E14 T29_RSENSE
R3655 1.0K 0 5% 1/16W MF LF 603
RBIAS E16 T29_RBIAS

=PP3V3_S0_T29P
R3690 3.3K 5% 1/16W MF LF 402
R3691 3.3K 5% 1/16W MF LF 402
C3690 1UF 10% 6.3V CERM 402
R3692 3.3K 5% 1/16W MF LF 402
R3623 10K 5% 1/16W MF LF 402
R3620 10K 5% 1/16W MF LF 402
Pull-ups required on GPIO1 & 2 if unused.
CLKREQ# not functional in endpoint mode.

CRITICAL
OMIT_TABLE
U3690
M95160
2KX8-1.8V
MLP
VCC
VSS
THM PAD
(T29_SPI_MOSI) D
(T29_SPI_CLK) C
(T29_SPI_CS_L) S_L
T29ROM_WP_L W_L
T29ROM_HOLD_L HOLD_L
(T29_SPI_MISO) Q
R3693 3.3K 5% 1/16W MF LF 402

T29_PCIE_CLKREQ_L P3 PCIE_CLKREQ_0*
T29_GPIO<1> (81) N4 PCIE_CLKREQ_1*
T29_GPIO<2> (81) M3 PCIE_CLKREQ_2*
T29_RSVD L4 PCIE_CLKREQ_3*
CLK REQUEST

T29_SPI_MOSI P1 EE_DI
T29_SPI_MISO M1 EE_DO
T29_SPI_CS_L N2 EE_CS*
T29_SPI_CLK L2 EE_CLK
EEPROM

T29_TP_THERM_DP A2 THERM_DP

T29_TEST_EN E4 TEST_EN
TP_T29_TEST_POINT_0 P5 TEST_POINT_0
TP_T29_TEST_POINT_1 N6 TEST_POINT_1
TP_T29_TEST_POINT_2 M5 TEST_POINT_2
TP_T29_TEST_POINT_3 L6 TEST_POINT_3
TEST PORT

R3625 0 5% 1/16W MF LF 402
R3629 0 5% 1/16W MF LF 402

TP_DP_T29SNK0_MLP<3> AA4 DPSNK0_ML_LANE_3P
TP_DP_T29SNK0_MLN<3> Y3 DPSNK0_ML_LANE_3N
TP_DP_T29SNK0_MLP<2> AA6 DPSNK0_ML_LANE_2P
TP_DP_T29SNK0_MLN<2> Y5 DPSNK0_ML_LANE_2N
TP_DP_T29SNK0_MLP<1> AA8 DPSNK0_ML_LANE_1P
TP_DP_T29SNK0_MLN<1> Y7 DPSNK0_ML_LANE_1N
TP_DP_T29SNK0_MLP<0> AA10 DPSNK0_ML_LANE_0P
TP_DP_T29SNK0_MLN<0> Y9 DPSNK0_ML_LANE_0N
TP_DP_T29SNK0_AUXCHP V1 DPSNK0_AUX_CHP
TP_DP_T29SNK0_AUXCHN W2 DPSNK0_AUX_CHN
TP_DP_T29SNK0_HPD V5 DPSNK0_HOT_PLUG_DET
SINK PORT 0

NC V9 DPSNK1_ML_LANE_3P
NC U8 DPSNK1_ML_LANE_3N
NC V11 DPSNK1_ML_LANE_2P
NC U10 DPSNK1_ML_LANE_2N
NC V13 DPSNK1_ML_LANE_1P
NC U12 DPSNK1_ML_LANE_1N
NC V15 DPSNK1_ML_LANE_0P
NC U14 DPSNK1_ML_LANE_0N
NC V7 DPSNK1_AUX_CHP
NC U6 DPSNK1_AUX_CHN
NC U4 DPSNK1_HOT_PLUG_DET
SINK PORT 1

DISPLAY

SOURCE PORT 0

DPSRC0_ML_LANE_3P AA18 DP_T29SRCA_ML_C_P<3>
DPSRC0_ML_LANE_3N Y17 DP_T29SRCA_ML_C_N<3>
DPSRC0_ML_LANE_2P AA16 DP_T29SRCA_ML_C_P<2>
DPSRC0_ML_LANE_2N Y15 DP_T29SRCA_ML_C_N<2>
DPSRC0_ML_LANE_1P AA14 DP_T29SRCA_ML_C_P<1>
DPSRC0_ML_LANE_1N Y13 DP_T29SRCA_ML_C_N<1>
DPSRC0_ML_LANE_0P AA12 DP_T29SRCA_ML_C_P<0>
DPSRC0_ML_LANE_0N Y11 DP_T29SRCA_ML_C_N<0>
DPSRC0_AUX_CHP W16 DP_T29SRCA_AUXCH_C_P
DPSRC0_AUX_CHN U16 DP_T29SRCA_AUXCH_C_N
DPSRC0_HOT_PLUG_DET V3 DP_T29SRCA_HPD

DP_ATEST Y19 T29_DP_ATEST
DP_RES_0 Y21
DP_RES_1 AA20 T29_DP_RES
R3685 14.0K 1% 1/16W MF LF 402
R3632 100K 5% 1/16W MF LF 402

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm
C3685 100PF 5% 50V CERM 402
C3686 0.01UF 10% 50V X7R 402

MISC

POWER ON RESET

PCIE_RST_0* K1 T29_PCIE_RESET_L<0>
PCIE_RST_1* J2 T29_PCIE_RESET_L<1>
PCIE_RST_2* K3 T29_PCIE_RESET_L<2>
PCIE_RST_3* J4 T29_PCIE_RESET_L<3>

JTAG

TDI T3 JTAG_T29P_TDI
TMS R4 JTAG_T29P_TMS
TCK R2 JTAG_T29P_TCK
TDO T1 JTAG_T29P_TDO

CLOCKS

REFCLK_100_IN_P H17 PCIE_CLK100M_T29_P
REFCLK_100_IN_N G16 PCIE_CLK100M_T29_N
XTAL_25_IN P17 SYSCLK_CLK25M_T29_R
XTAL_25_OUT R16 TP_T29_XTAL25OUT
TMU_CLK_OUT U2 T29_TMU_CLK_OUT
TMU_CLK_IN E2 T29_TMU_CLK_IN

=PP3V3_S0_T29P
R3698 10K 5% 1/16W MF LF 402
R3695 806 1% 1/16W MF LF 402
SYSCLK_CLK25M_T29
R3696 1K 5% 1/16W MF LF 402
NO STUFF
R3699 10K 5% 1/16W MF LF 402

PORTS

PORT2

PRT2_T29T_P A14 T29_R2D_C_P<0>
PRT2_T29T_N A12 T29_R2D_C_N<0>
PRT2_T29R_P C12 T29_D2R_P<0>
PRT2_T29R_N C10 T29_D2R_N<0>
T29_2_LSEO G4 T29_LSEO<0>
T29_2_LSOE H3 T29_LSOE<0>
MDP PORT A - LINK 0

PORT3

PRT3_T29T_P A18 T29_R2D_C_P<1>
PRT3_T29T_N A16 T29_R2D_C_N<1>
PRT3_T29R_P C16 T29_D2R_P<1>
PRT3_T29R_N C14 T29_D2R_N<1>
T29_3_LSEO G2 T29_LSEO<1>
T29_3_LSOE H1 T29_LSOE<1>
MDP PORT A - LINK 1

CABLE PORT - LINK 0

T29_R2C_C_P<0> A6 PRT0_T29T_P
T29_R2C_C_N<0> A4 PRT0_T29T_N
T29_C2R_P<0> C4 PRT0_T29R_P
T29_C2R_N<0> C2 PRT0_T29R_N
T29_R2C_LSEO<0> J6 T29_0_LSEO
T29_C2R_LSEO<0> K5 T29_0_LSOE
PORT0

CABLE PORT - LINK 1

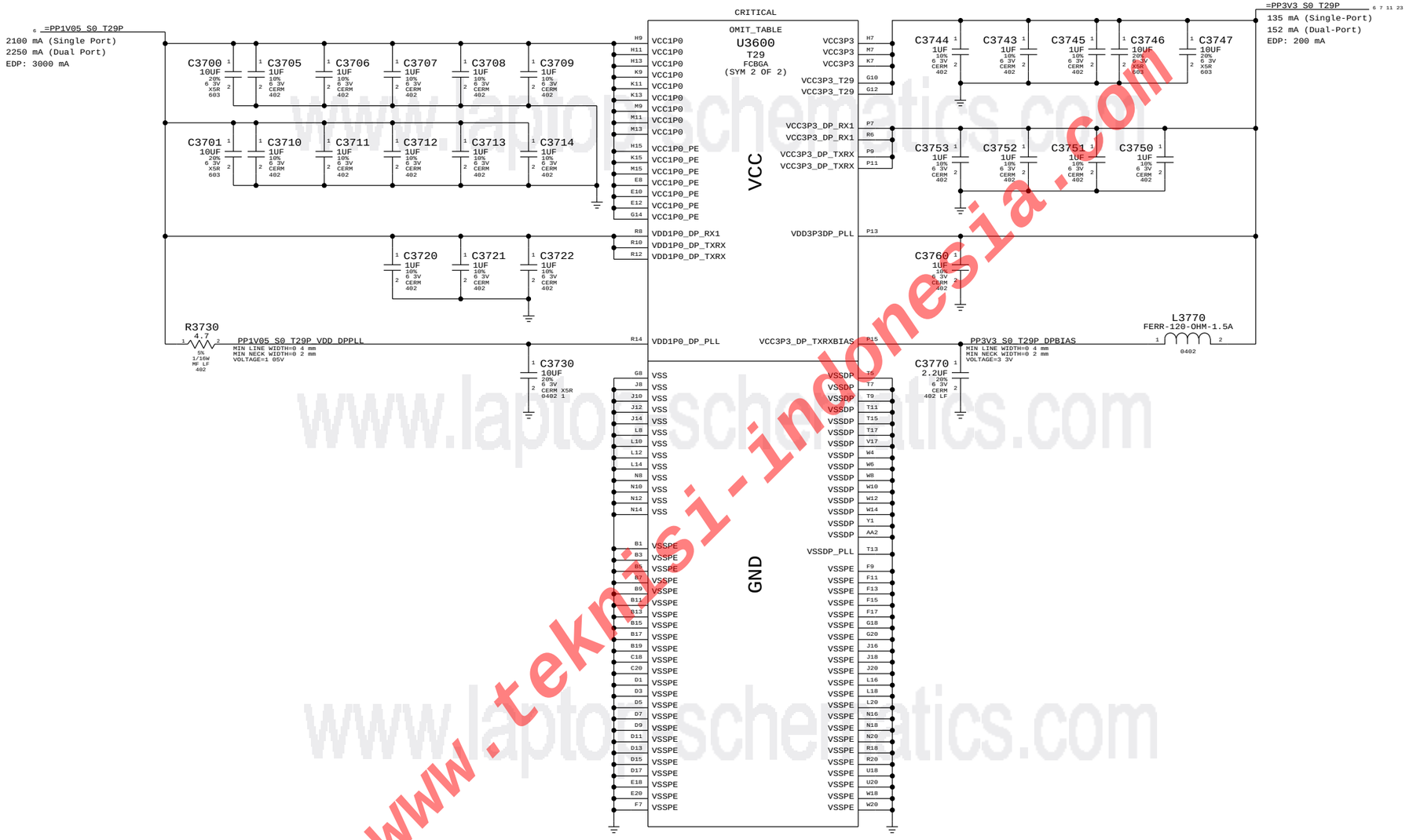
T29_R2C_C_P<1> A10 PRT1_T29T_P
T29_R2C_C_N<1> A8 PRT1_T29T_N
T29_C2R_P<1> C8 PRT1_T29R_P
T29_C2R_N<1> C6 PRT1_T29R_N
T29_R2C_LSEO<1> G6 T29_1_LSEO
T29_C2R_LSEO<1> H5 T29_1_LSOE
PORT1

I2C_T29_SDA F3 T29_SDA
I2C_T29_SCL F5 T29_SCL

NOTE: C2R = Cable to Router
R2C = Router to Cable

T29_R2C_LSEO<0> =T29_R2C_LSEO<0>
T29_C2R_LSEO<0> =T29_C2R_LSEO<0>
T29_LSEO<0> =T29_LSEO<0>
T29_LSOE<0> =T29_LSOE<0>
MAKE BASE=TRUE

SYNC_MASTER=T29_D SYNC_DATE=11/01/2010
PAGE TITLE: T29 Primary (1 of 2)
Apple Inc.
DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 36 OF 110
SHEET 23 OF 48



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_D SYNC_DATE=03/17/2011

PAGE TITLE: T29 Primary (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

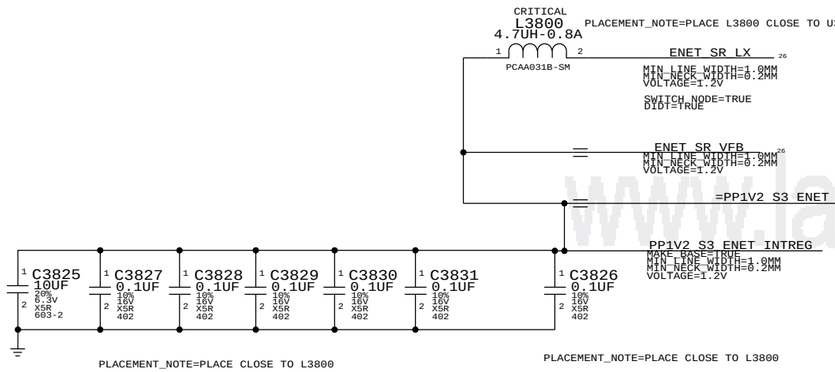
REVISION: C.0.0

BRANCH:

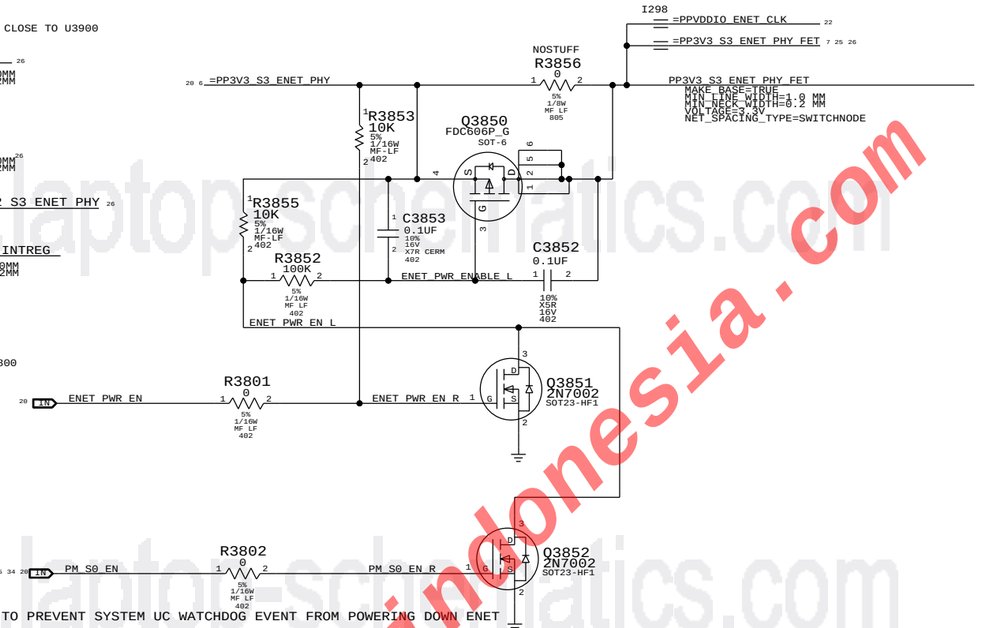
PAGE: 37 OF 110

SHEET: 24 OF 48

CAESAR IV 1.2V INT.VR CMPTS

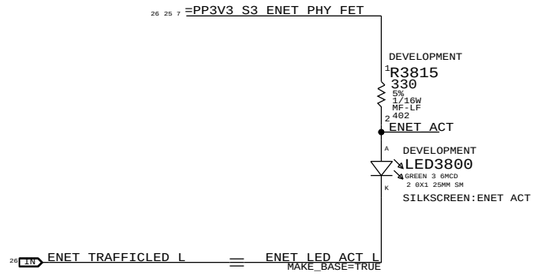


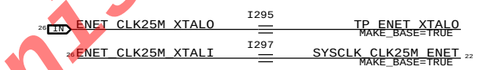
CAESAR IV POWER ENABLE CIRCUIT



ADDED TO PREVENT SYSTEM UC WATCHDOG EVENT FROM POWERING DOWN ENET

CAESAR IV ACTIVITY LED





SYNC_MASTER=K62 SYNC_DATE=09/16/2010

PAGE TITLE: CAESAR IV SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 38 OF 110

SHEET: 25 OF 48

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)

=PP3V3_S3_ENET_PHY_FET

C3979 4.7UF 20% 6.3V CERM 603

R3901 0 5% 1/16W MF LF 402 — ENET_3V3_S3_SR_IN
SWITCH_NODE=TRUE
DIDT=TRUE
NET_SPACING_TYPE=SWITCHNODE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C3980 0.1UF 10% 16V X5R 402
C3981 0.1UF 10% 16V X5R 402

CRITICAL
L3900 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3900 0.1UF 10% 16V X7R CERM 402

R3900 0 5% 1/16W MF LF 402 — ENET_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

CRITICAL
L3905 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3905 0.1UF 10% 16V X7R CERM 402

CRITICAL
L3910 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF LF 402
C3910 0.1UF 10% 16V X7R CERM 402
C3911 0.1UF 10% 16V X7R CERM 402

R3942 IS A LEAKAGE PATH, SO RESISTOR VALUE IS SMALL.

20 =PP3V3_S0_ENET_PHY

Current Limiting Resistor: R3942 4.7K 5% 1/16W MF LF 402

NOSTUFF R3998 0 5% 1/16W MF LF 402 — 20 IN ENET_VMAIN_CTRL

R3940 4.7K 5% 1/16W MF LF 402
R3941 4.7K 5% 1/16W MF LF 402

C3917 0.1UF 10% 16V X7R CERM 402
C3918 0.1UF 10% 16V X7R CERM 402
C3915 4.7UF 10% 6.3V X5R CERM 603
C3916 0.1UF 10% 16V X7R CERM 402

ENET_SR_LX 25
ENET_SR_VFB 25

Internal 1.2V Switching Regulator pins.

=PP1V2_S3_ENET_PHY 25
396mA (1000base-T, Caesar II)

CRITICAL
L3920 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3921 0.1UF 10% 16V X7R CERM 402
C3920 4.7UF 10% 6.3V X5R CERM 603

CRITICAL
L3925 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3926 0.1UF 10% 16V X7R CERM 402
C3925 4.7UF 10% 6.3V X5R CERM 603

CRITICAL
L3930 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3931 0.1UF 10% 16V X7R CERM 402
C3930 4.7UF 10% 6.3V X5R CERM 603

C3936 0.1UF 10% 16V X7R CERM 402
C3935 10UF 10% 6.3V X5R 805

Pin	Net
30	AVDDH
36	AVDDH
25	BIASVDDH
12	XTALVDDH
42	VDDO
9	SR_VDD
10	SR_VDDP
11	SR_LX
8	SR_VFB
27	AVDDL
33	AVDDL
39	AVDDL
18	PCIE_PLLVDDL
21	PCIE_PLLVDDL
24	GPHY_PLLVDDL
15	VDDC
41	VDDC

OMIT_TABLE
U3900 BCM57761A0KMLG QFN

Pin	Net
40	VMAIN_PRSNT (IPD ENET)
16	PCIE_TXD_N
17	PCIE_TXD_P
22	PCIE_RXD_P
23	PCIE_RXD_N
20	PCIE_REFCLK_P
19	PCIE_REFCLK_N
6	PERST* (IPD)
7	CLKREQ* (OD)
1	WAKE* (OD)
2	LOW_PWR (IPD)
4	SMB_CLK
5	SMD_DATA (IPD ENETM)
46	SCLK/SPD1000LED*
44	SI*/EEDATA
45	SO*/LINKLED*
43	CS*/EECLK
48	SPD100LED* (OD)
47	TRAFFICLED* (OD)
13	XTALI
14	XTALO
26	RDAC
49	THRM_PAD

(IPU)

Pin	Net
28	TRD0_P — ENETCONN_MDI_P<0>
29	TRD0_N — ENETCONN_MDI_N<0>
32	TRD1_P — ENETCONN_MDI_P<1>
31	TRD1_N — ENETCONN_MDI_N<1>
34	TRD2_P — ENETCONN_MDI_P<2>
35	TRD2_N — ENETCONN_MDI_N<2>
38	TRD3_P — ENETCONN_MDI_P<3>
37	TRD3_N — ENETCONN_MDI_N<3>
3	GPIO_0 — ENET_WOL_ENABLE

ENET_WAKE:GPIO R3999 0 5% 1/16W MF LF 402 — ENET_WAKE_L

C3950 0.1uF — PCIE_ENET_D2R_N
C3951 0.1uF — PCIE_ENET_D2R_P
C3955 0.1uF — PCIE_ENET_R2D_C_P
C3956 0.1uF — PCIE_ENET_R2D_C_N

ENET_WAKE:PCIE R3943 0 5% 1/16W MF LF 402 — =ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
ENET_WAKE_R_L
ENET_LOW_PWR
ENET_SMB_CLK
ENET_SMB_DATA
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
TP_ENET_SPD100LED_L
ENET_TRAFFICLED_L
ENET_CLK25M_XTALI
ENET_CLK25M_XTALO
ENET_RDAC

R3965 1.24K 1% 1/16W MF LF 402

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_S3_ENET_PHY_FET

R3993 4.7K 5% 1/16W MF LF 402
R3992 4.7K 5% 1/16W MF LF 402
R3904 0 5% 1/16W MF LF 402

U3990 M45PE10 SOIC OMIT_TABLE
VCC, VSS, C, S*, W*, RESET*, D, Q

C3990 0.1UF 10% 16V X7R CERM 402

ENET_SCLK — ENET_SCLK_R
ENET_CS_L
ENET_SWP_L
ENET_SRESET_L
ENET_MOSI
ENET_MISO

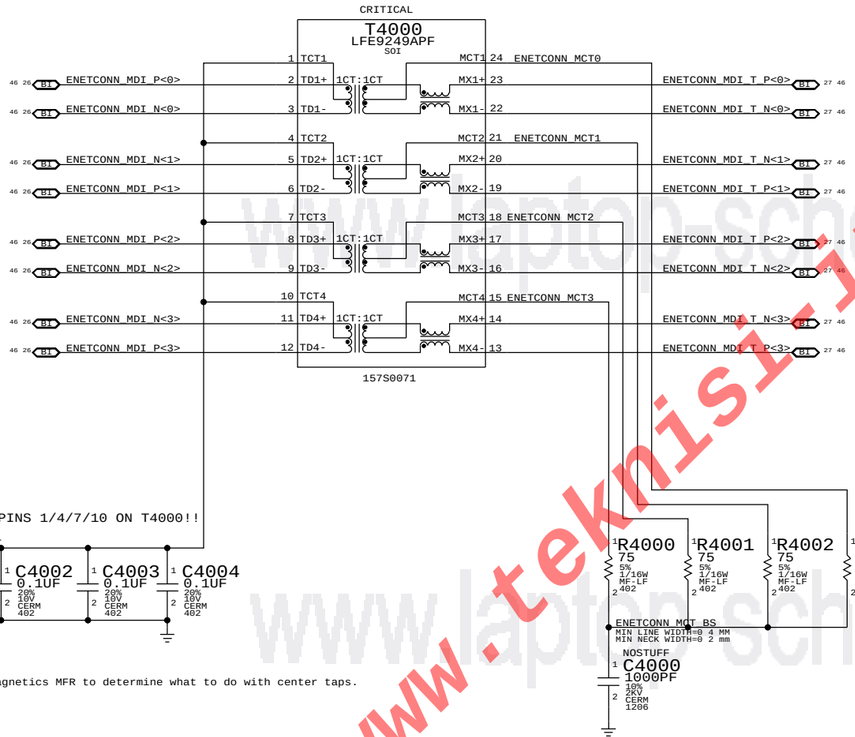
NOSTUFF R3990 4.7K 5% 1/16W MF LF 402
R3997 4.7K 5% 1/16W MF LF 402

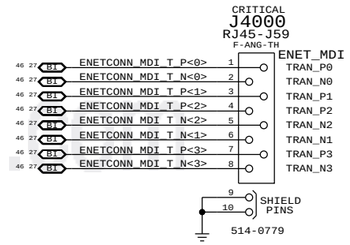
NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=TONY
SYNC_DATE=10/01/2010
PAGE TITLE: ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-8774
SIZE D
REVISION C.0.0
BRANCH
PAGE 39 OF 110
SHEET 26 OF 48



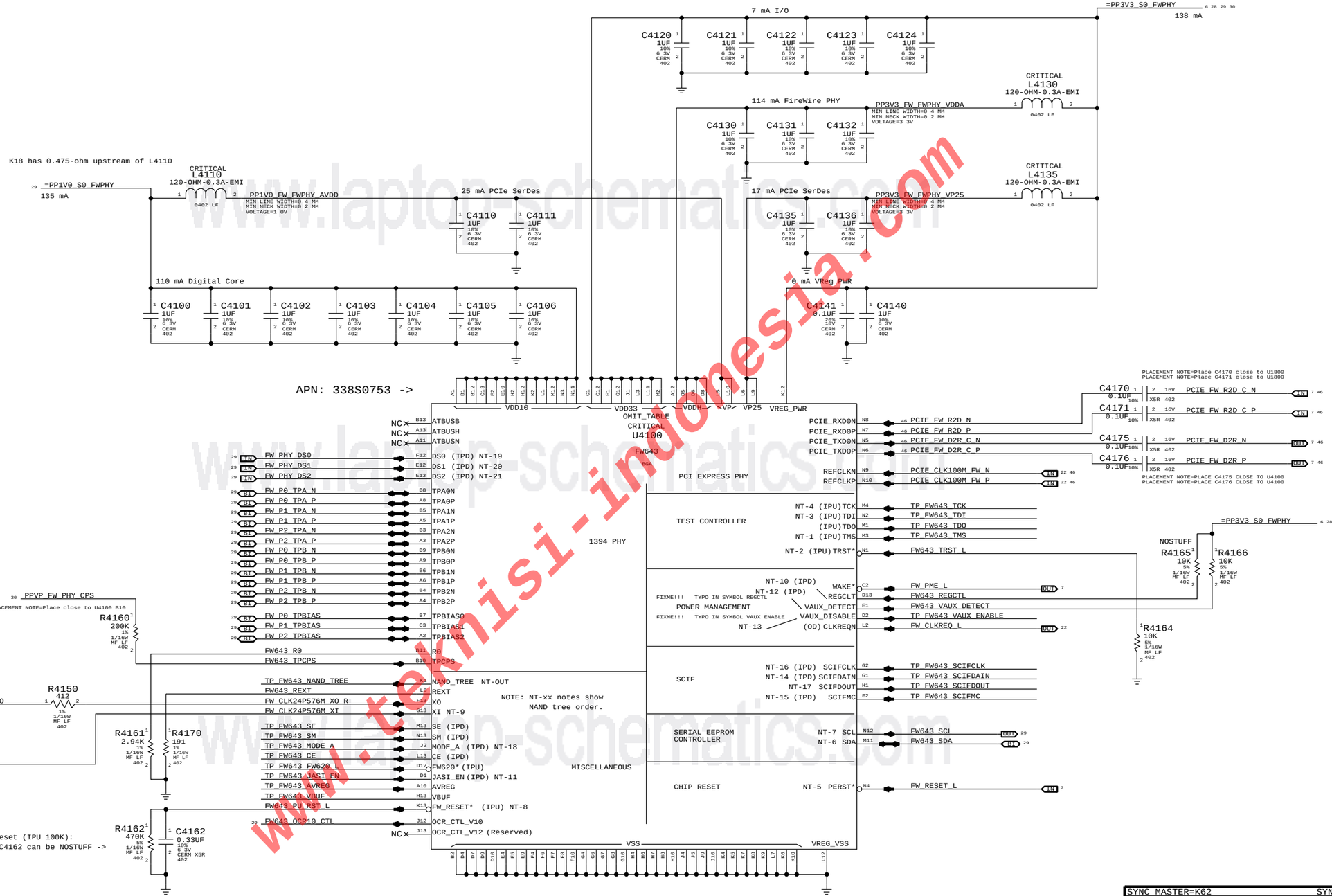


SYNC_MASTER=K62 SYNC_DATE=09/16/2010

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 40 OF 110
SHEET: 27 OF 48



SYNC_MASTER=K62 SYNC_DATE=09/09/2010

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

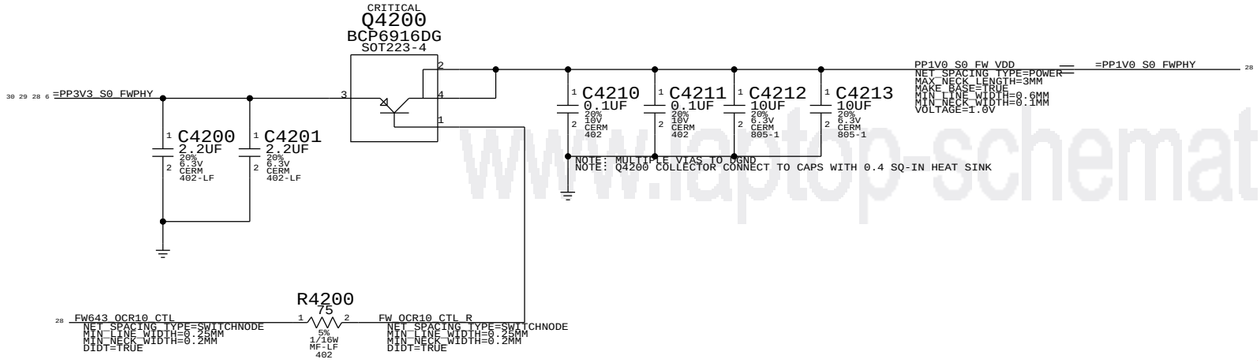
REVISION C.0.0

BRANCH

PAGE 41 OF 110

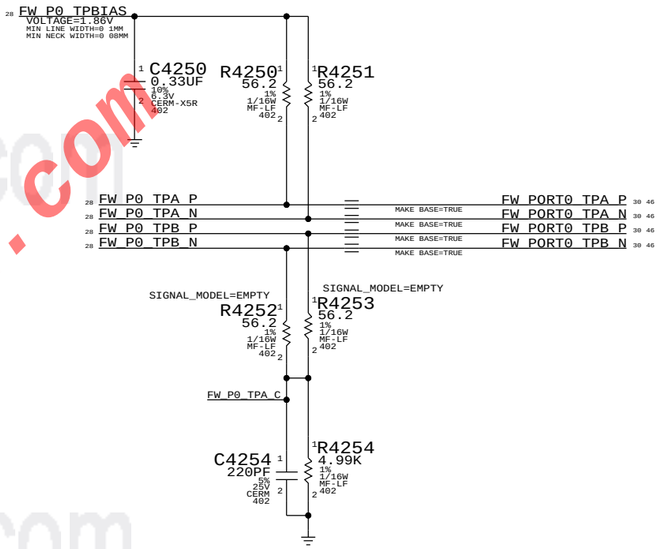
SHEET 28 OF 48

FW643 1.0V GENERATION

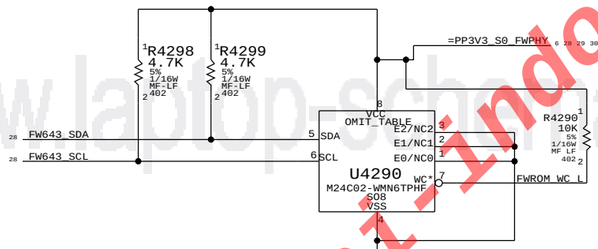


Termination

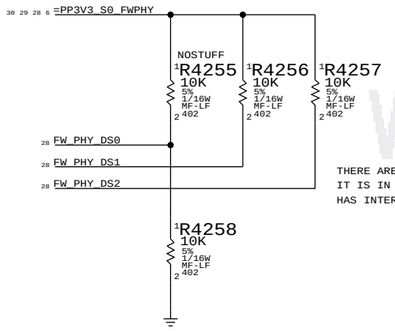
Place close to FireWire PHY



FW643 GUID ROM



1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

2ND & 3RD TPA/TPB PAIR UNUSED

FW_P1_TPBIAS	—	NC_FW_PORT1_TPBIAS (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P1_TPA_P	—	NC_FW_PORT1_TPA_P (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P1_TPA_N	—	NC_FW_PORT1_TPA_N (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P1_TPB_P	—	NC_FW_PORT1_TPB_P (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P1_TPB_N	—	NC_FW_PORT1_TPB_N (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P2_TPBIAS	—	NC_FW_PORT2_TPBIAS (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P2_TPA_P	—	NC_FW_PORT2_TPA_P (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P2_TPA_N	—	NC_FW_PORT2_TPA_N (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P2_TPB_P	—	NC_FW_PORT2_TPB_P (MAKE BASE=TRUE, NO TEST=TRUE)
FW_P2_TPB_N	—	NC_FW_PORT2_TPB_N (MAKE BASE=TRUE, NO TEST=TRUE)

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

SYNC_MASTER=K62 SYNC_DATE=09/23/2010

PAGE TITLE: FireWire: 1394B MISC

Apple Inc.

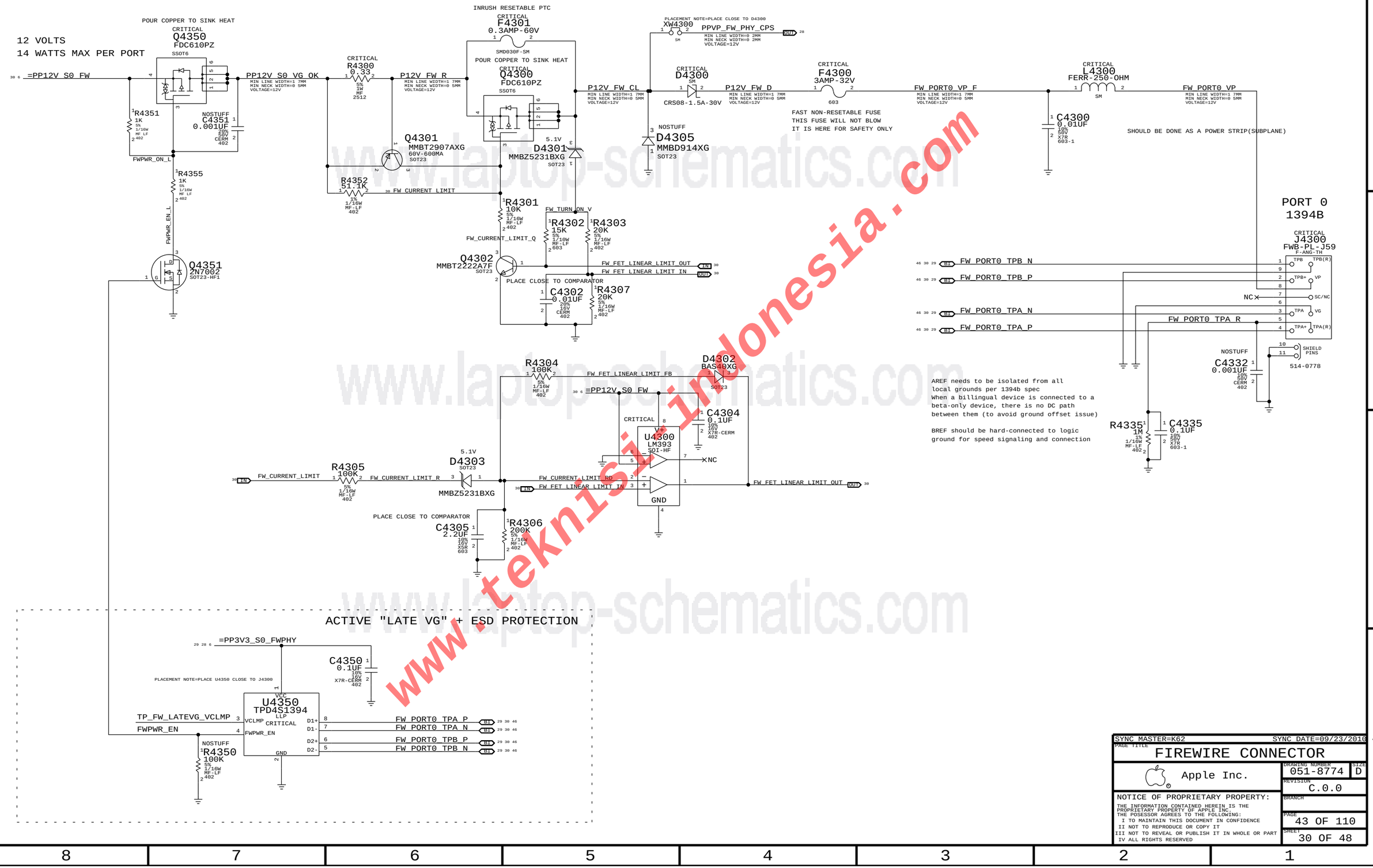
DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 42 OF 110

SHEET: 29 OF 48



USB 7-PORT HUB

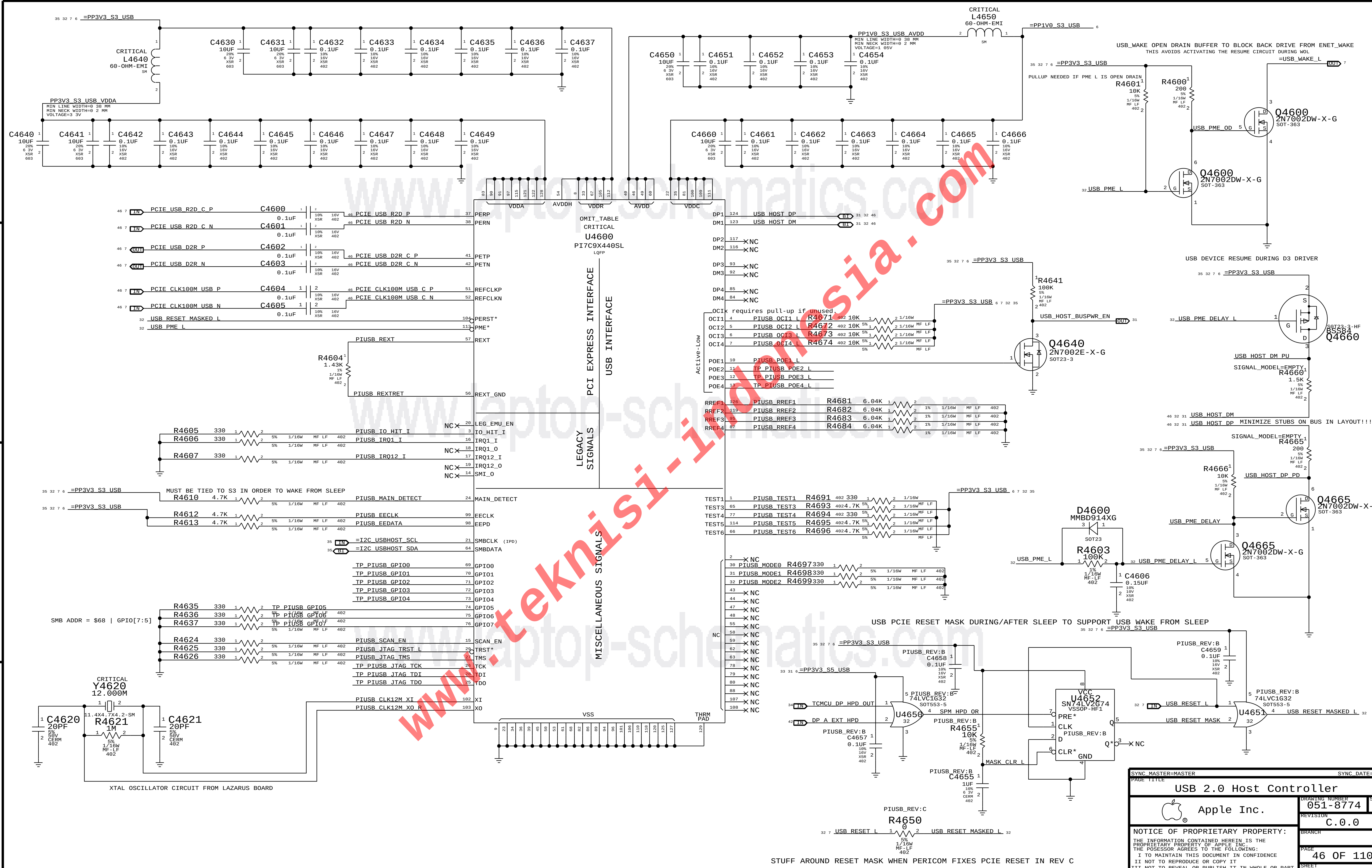
SYNC MASTER=K59 SYNC DATE=11/01/2010
PAGE TITLE

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 45 OF 110
SHEET 31 OF 48

USB DEV CONNECTOR

DEVELOPMENT CONNECTOR USB MUX



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: USB 2.0 Host Controller

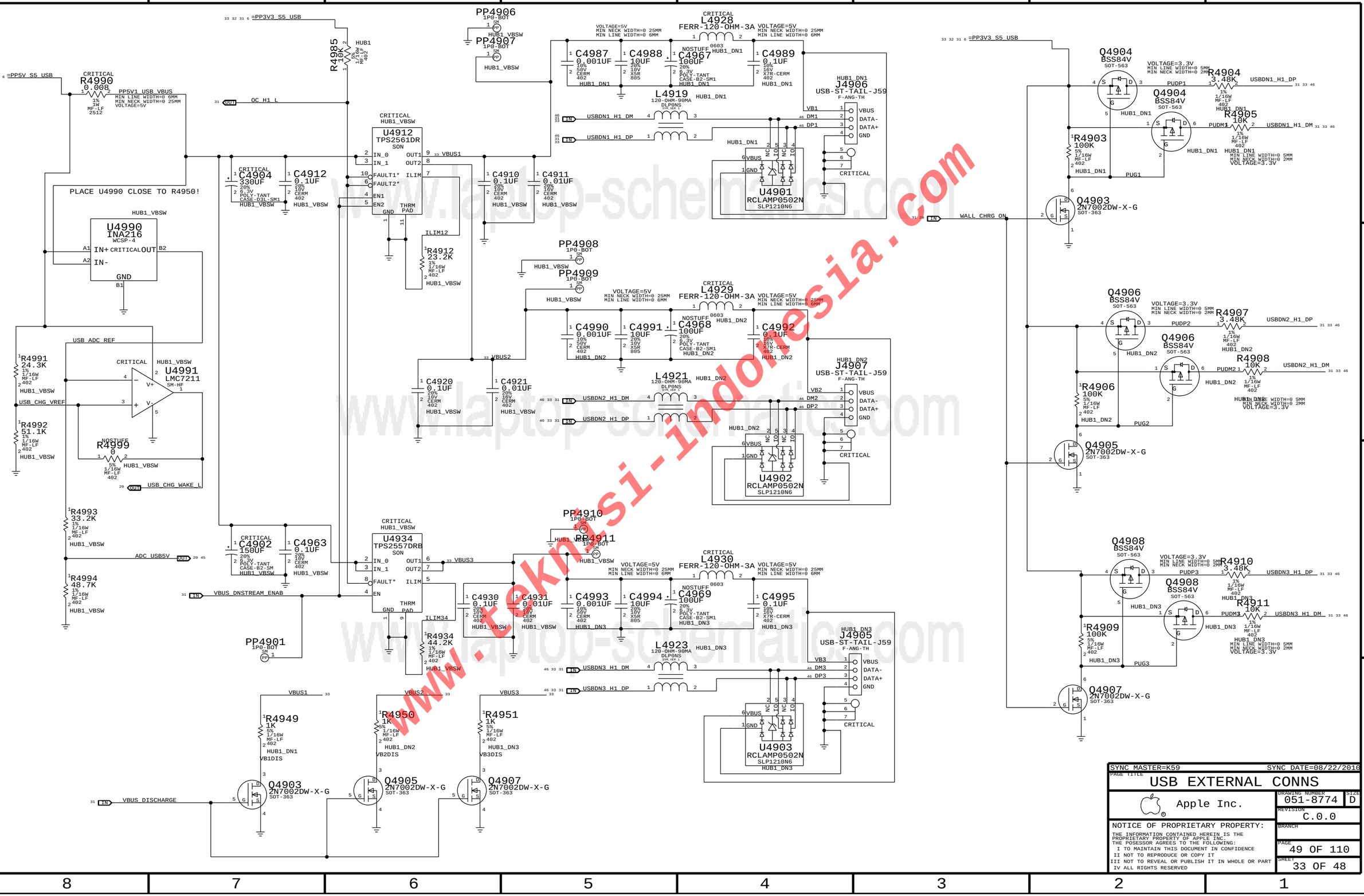
Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

PAGE: 46 OF 110

SHEET: 32 OF 48



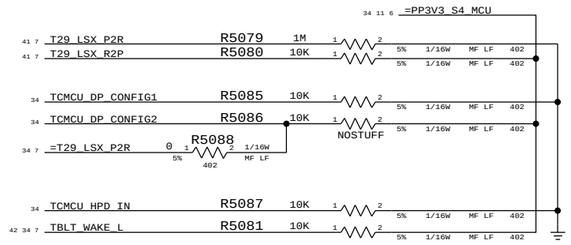
SYNC MASTER=K59	SYNC DATE=08/22/2010
PAGE TITLE	USB EXTERNAL CONNS
Apple Inc.	DRAWING NUMBER 051-8774 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 49 OF 110
	SHEET 33 OF 48

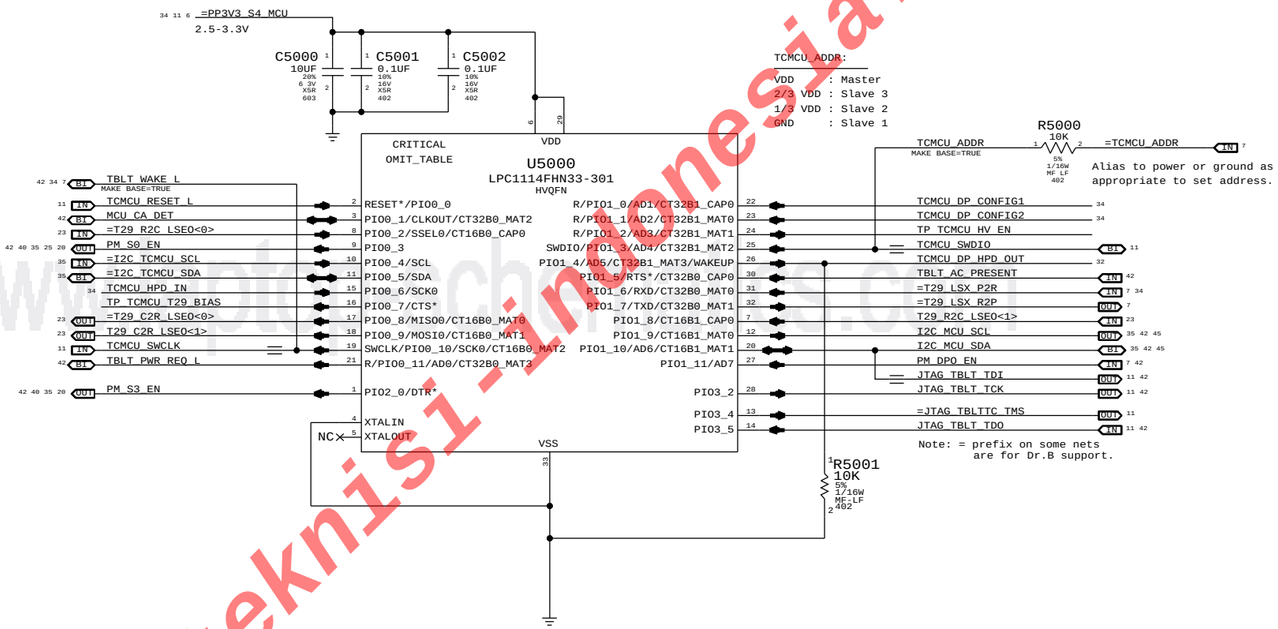
MCU Pull-ups/downs

T29 host/device has 10K pull-up on LSX_R2P.
Dual-plug cable has cross-over for P2R/R2P.

Device micro (U5000) senses pull-up to detect host. Cable may be powered-off until host pull-up is detected.

P2R = Plug to Receptacle
R2P = Receptacle to Plug





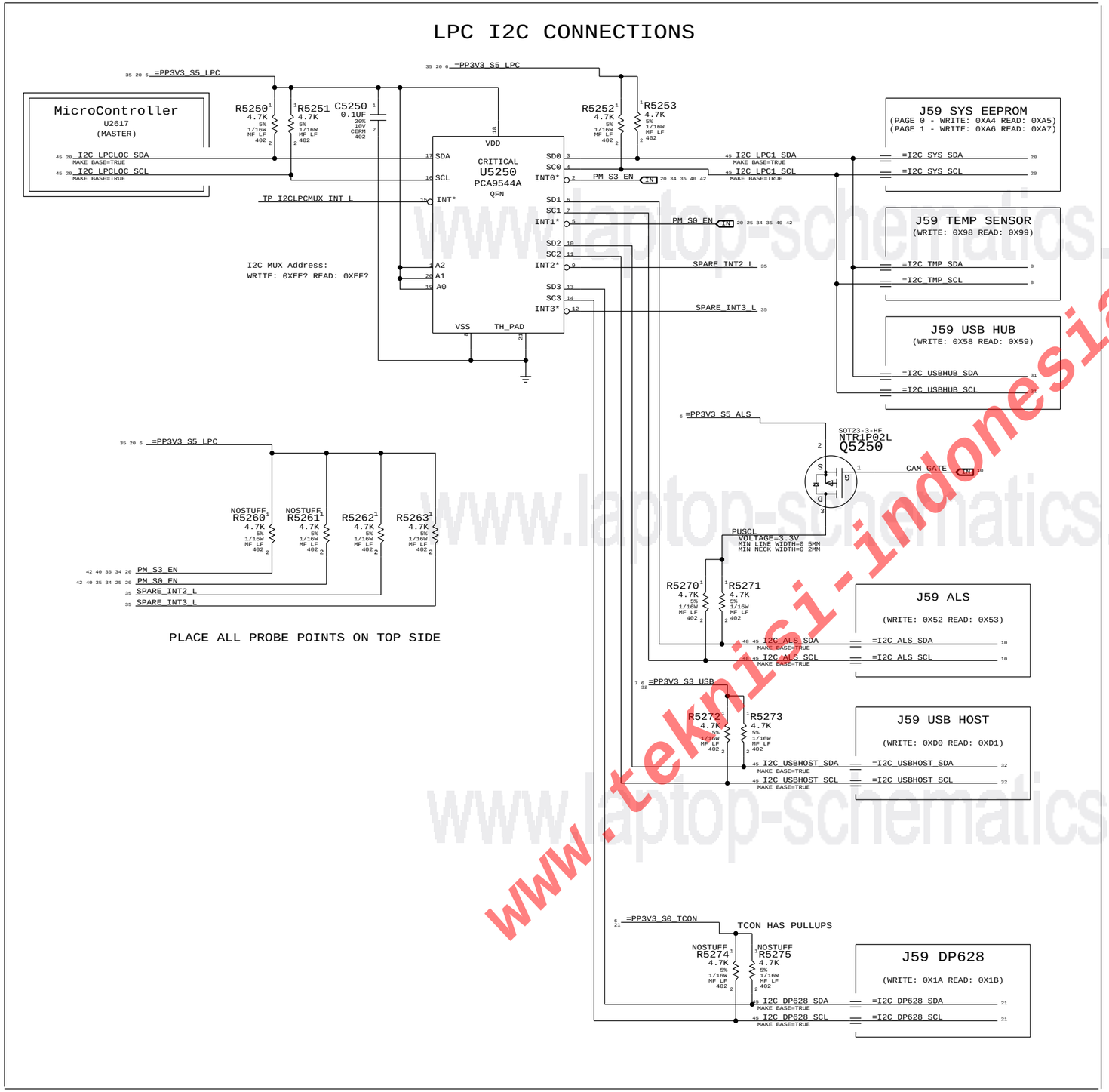
SYNC_MASTER=T29_D SYNC_DATE=03/17/2013

PAGE TITLE: Tethered Cable MCU

Apple Inc.

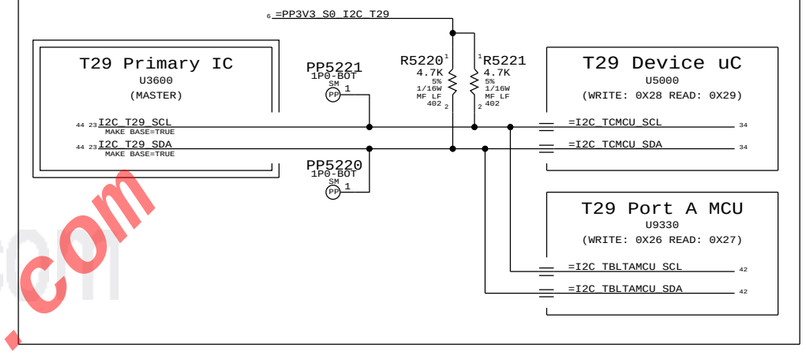
DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 50 OF 110
SHEET: 34 OF 48

LPC I2C CONNECTIONS



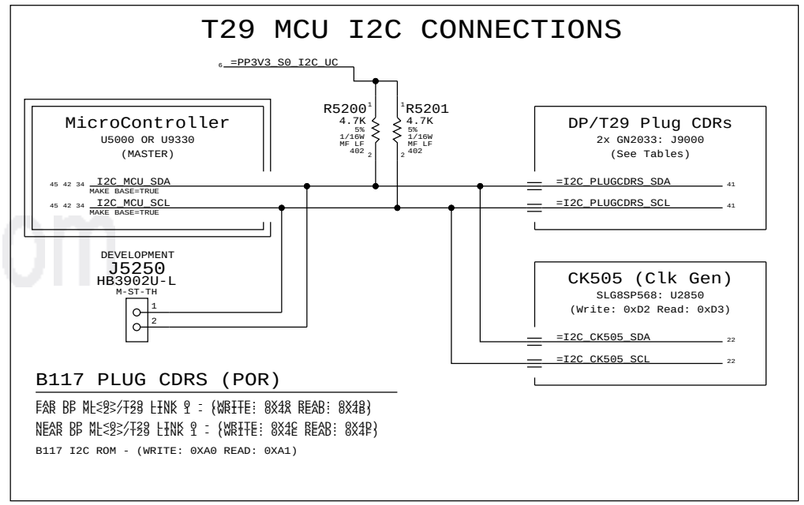
PLACE ALL PROBE POINTS ON TOP SIDE

T29 IC I2C Connections



PLACE ALL I2C PROBE POINTS ON TOP SIDE

T29 MCU I2C CONNECTIONS



B117 PLUG CDRS (POR)

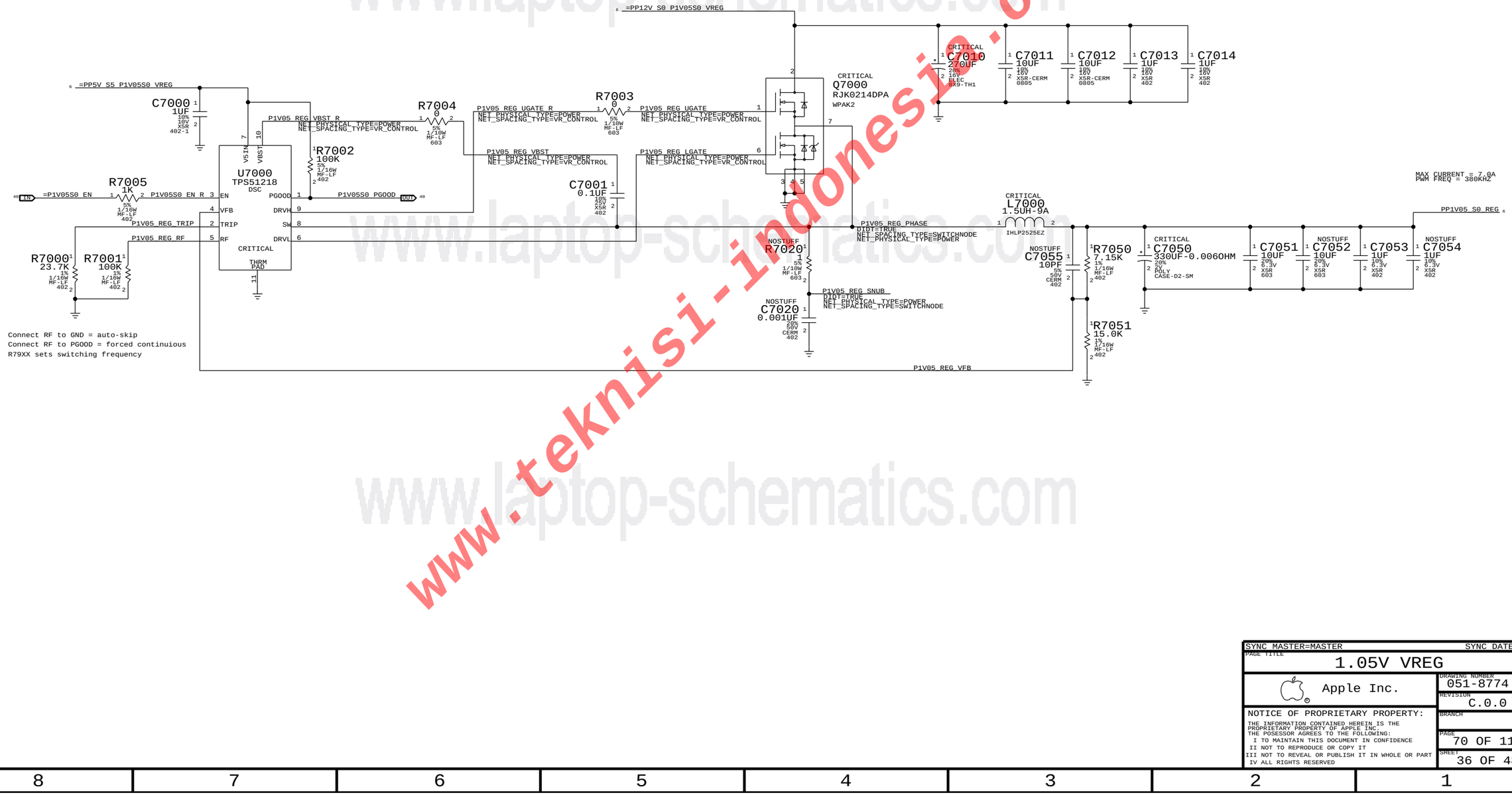
FAR DP ML<0>/T29 LINK 0 - (WRITE: 0X18 READ: 0X19)
NEAR DP ML<0>/T29 LINK 0 - (WRITE: 0X1E READ: 0X1F)
B117 I2C ROM - (WRITE: 0XA0 READ: 0XA1)

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
J59 & T29 SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 52 OF 110
SHEET 35 OF 48



SYNC MASTER=MASTER SYNC DATE=N/A

PAGE TITLE
1.05V VREG

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 70 OF 110
SHEET 36 OF 48

Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP15V_T29_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
T29BST - Stuffs 15V boost regulator

T29 15V Boost Regulator

8-13V Input
Changes required
for 2S.

=PPVIN_SW_T29BST

CRITICAL
T29BST
Q7180
SI8409DB
80A

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_T29BST
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm

Voltage not specified here
add property on another page

T29BST R7180 470K 5% 1/16W MF LF 402
T29BST C7180 0.1UF 10% 50V X7R 603 1
T29BST_PWREN_DIV_L
T29BST R7181 330K 5% 1/16W MF LF 402

T29BST_PWREN_L

T29BST Q7105 SSM3K15FV SOD VESM HF

T29_A_HV_EN

T29BST R7191 200K 1% 1/16W MF LF 402 <R1>
T29BST C7190 10UF 10% 25V X5R 805
T29BST C7191 10UF 10% 25V X5R 805

CRITICAL
T29BST
L7195
10UH-4A-68-MOHM
PCMB063T 100MS

T29BST_BOOST
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
SWITCH NODE=TRUE
DIDT=TRUE

CRITICAL
T29BST
U7190
LT3957
QFN

VIN
SW
EN/UVLO
INTVCC
VC
RT
SS
SYNC
SNS1
SNS2
NC
FBX
SGND
GND

T29BST_EN_UVLO
T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS
T29BST_VC_RC
T29BST_FBX

T29BST C7192 4.7UF 10% 16V X5R 805
T29BST C7187 47PF 5% 50V CERM 402
T29BST R7193 10K 1% 1/16W MF LF 402
T29BST R7192 73.2K 1% 1/16W MF LF 402 <R2>
T29BST C7193 0.033UF 10% 16V XSR 402
T29BST R7194 41.2K 1% 1/16W MF LF 402
T29BST C7194 0.33UF 10% 6.3V CERM X5R 402

GND_T29BST_SGND
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to
GND inside package,
no XW necessary.

T29BST_SNS1
T29BST_SNS2
T29BST_VSNS

T29BST R7189 0 5% 1/16W MF LF 402
CRITICAL
T29BST
D7195
POWERDI 123
DFLS230L

XW7195
SM
PLACE NEAR=C7195 1 2 mm

T29BST C7188 10PF 5% 50V CERM 402
T29BST R7195 137K 1% 1/16W MF LF 402 <Ra>
NO STUFF
T29BST C7189 100PF 5% 50V CERM 402
T29BST R7196 15.8K 1% 1/16W MF LF 402 <Rb>

Vout = 1.6V * (1 + Ra / Rb)

T29BST C7195 4.7UF 10% 50V X7R CERM 1206
T29BST C7196 4.7UF 10% 50V X7R CERM 1206
T29BST C7197 4.7UF 10% 50V X7R CERM 1206
T29BST C7198 4.7UF 10% 50V X7R CERM 1206
T29BST C7199 0.001UF 10% 50V X7R 402

=PP15V_T29_REG
Vout = 15.47V
Max Current = 1A
Freq = 300KHz

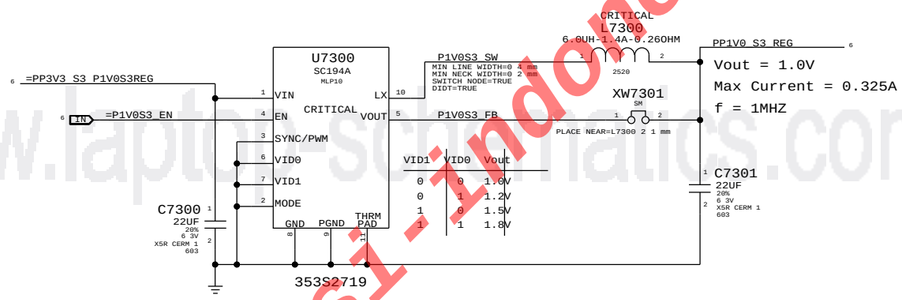
SYNC_MASTER=T29_D SYNC_DATE=03/17/2011

PAGE TITLE
Power: T29 15V Boost

Apple Inc.

DRAWING NUMBER 051-8774
SIZE D
REVISION C.0.0
BRANCH
PAGE 71 OF 110
SHEET 37 OF 48

1.0V Switcher



SYNC MASTER=MASTER	SYNC_DATE=N/A
PAGE TITLE: Power: USB (1.0V S3)	
Apple Inc.	DRAWING NUMBER: 051-8774 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 73 OF 110
	SHEET: 38 OF 48

5V_S3/3.3V_S5 POWER SUPPLY

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0927	1	FDMC3020DC	Q7760	CRITICAL	
376S0928	1	FDMC2514SDC	Q7761	CRITICAL	

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2

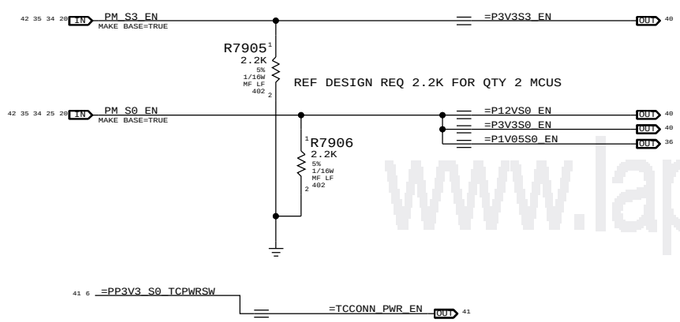
MAX CURRENT = 7.0A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 7.0A

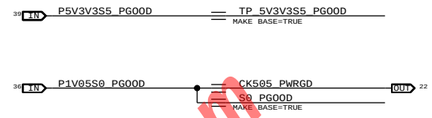
SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3

SYNC MASTER=MASTER	SYNC DATE=N/A
PAGE TITLE	5V/3.3V SUPPLY
Apple Inc.	DRAWING NUMBER 051-8774 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 77 OF 110
	SHEET 39 OF 48

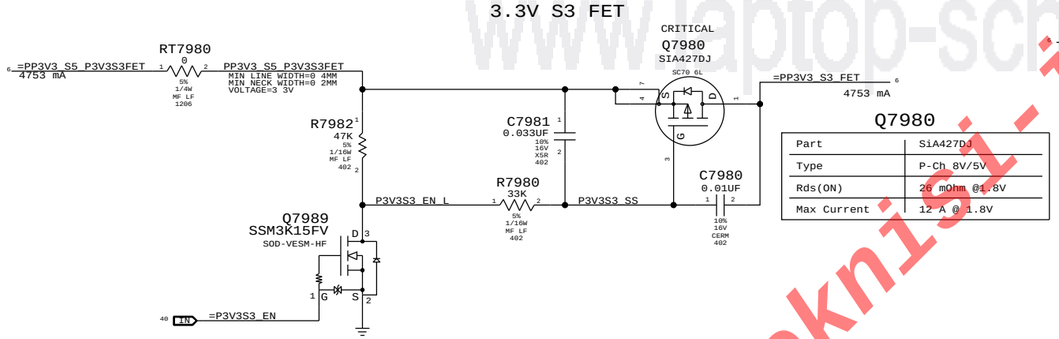
T29 / Device Rails



Power Goods



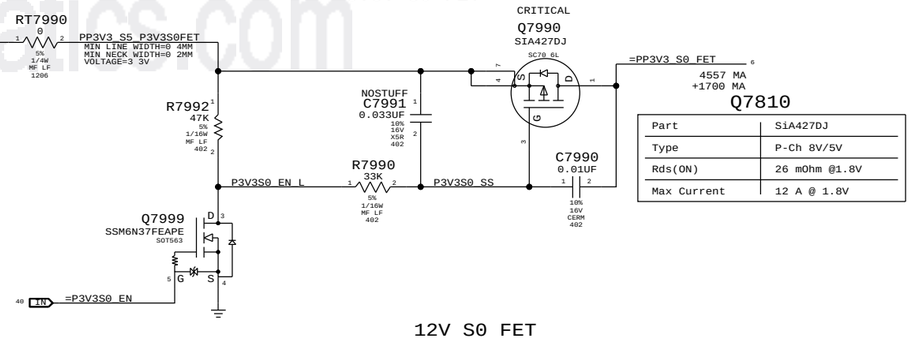
3.3V S3 FET



Q7980

Part	SiA427DJ
Type	P-Ch 8V/5V
Rds(ON)	26 mOhm @1.8V
Max Current	12 A @ 1.8V

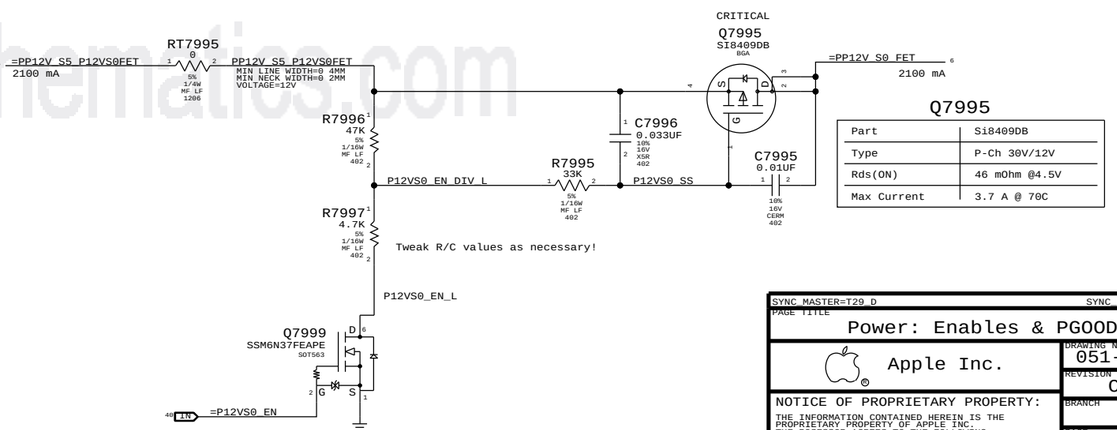
3.3V S0 FET



Q7810

Part	SiA427DJ
Type	P-Ch 8V/5V
Rds(ON)	26 mOhm @1.8V
Max Current	12 A @ 1.8V

12V S0 FET



Q7995

Part	Si8409DB
Type	P-Ch 30V/12V
Rds(ON)	46 mOhm @4.5V
Max Current	3.7 A @ 70C

SYNC_MASTER=T29_D SYNC_DATE=09/30/2010

PAGE TITLE

Power: Enables & PGOODs

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

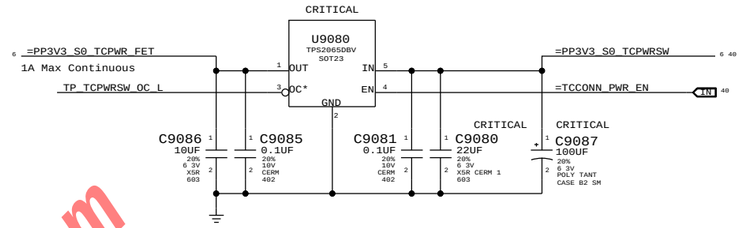
REVISION C.0.0

BRANCH

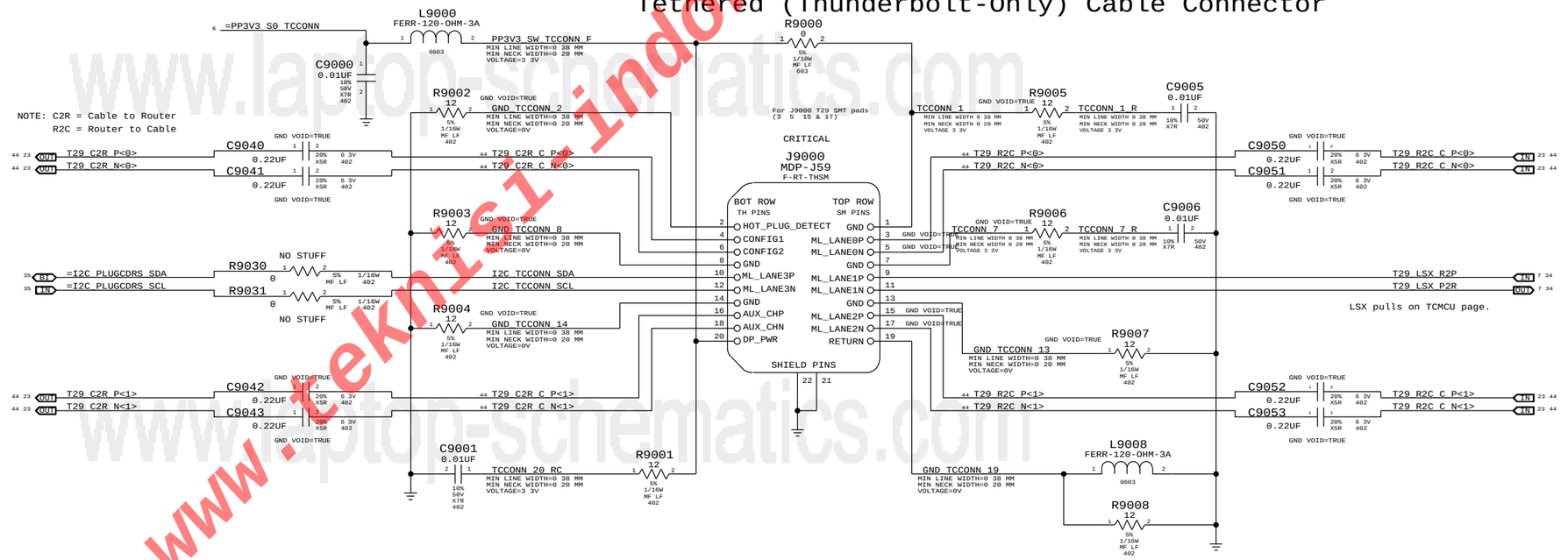
PAGE 79 OF 110

SHEET 40 OF 48

Cable 3.3V Power Switch



Tethered (Thunderbolt-Only) Cable Connector



SYNC_MASTER=T29_D SYNC_DATE=03/17/2013

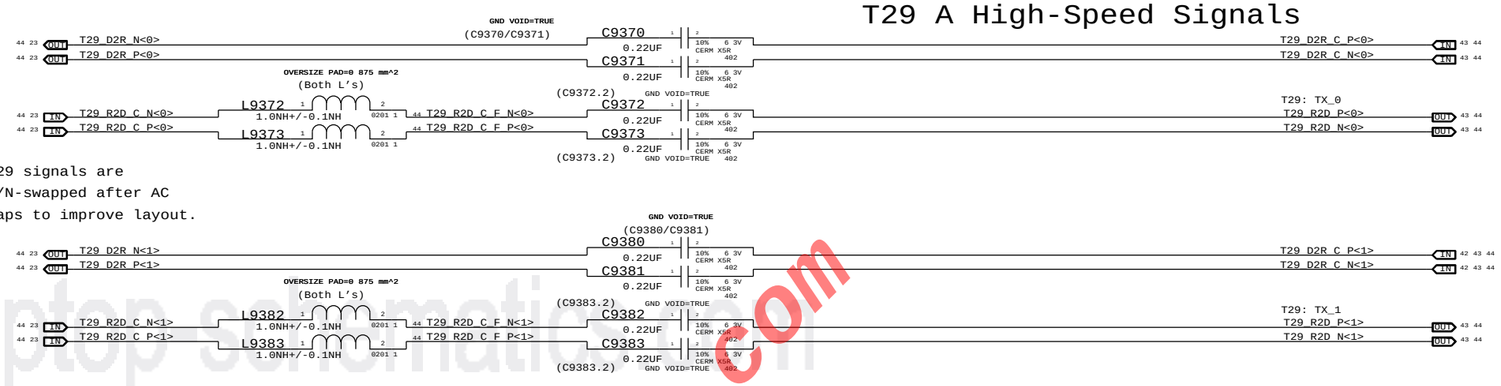
PAGE TITLE: Tethered Cable Connector

Apple Inc.

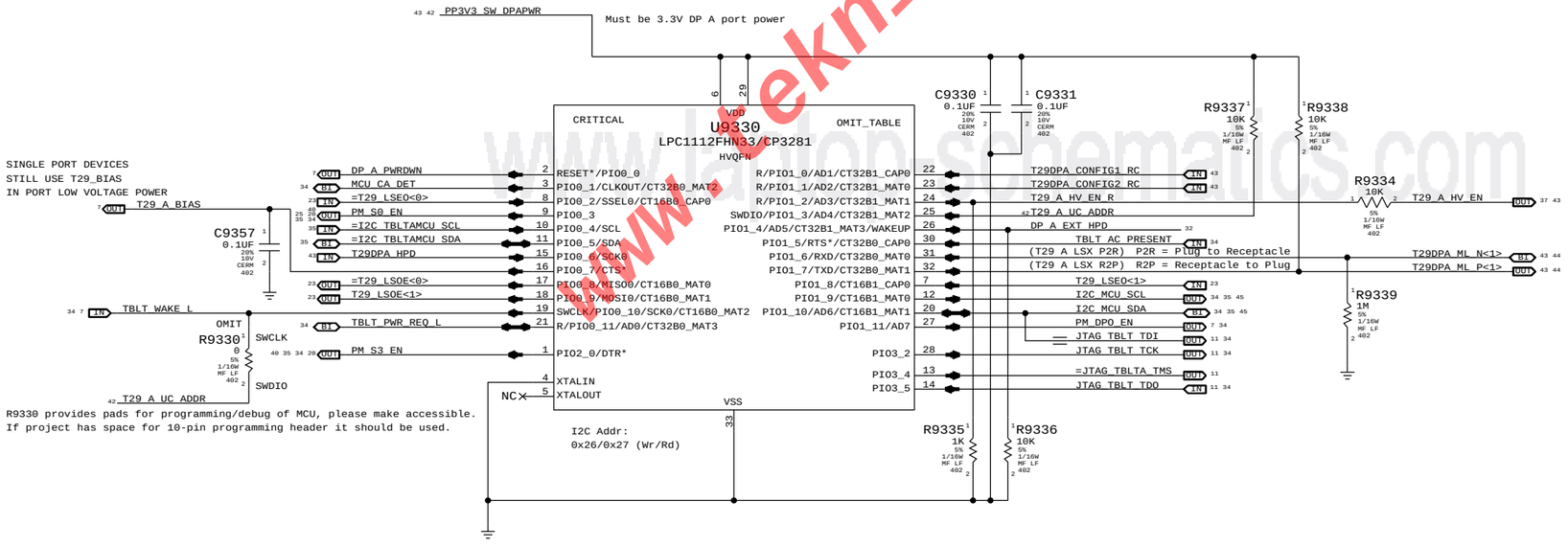
DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 90 OF 110
SHEET: 41 OF 48

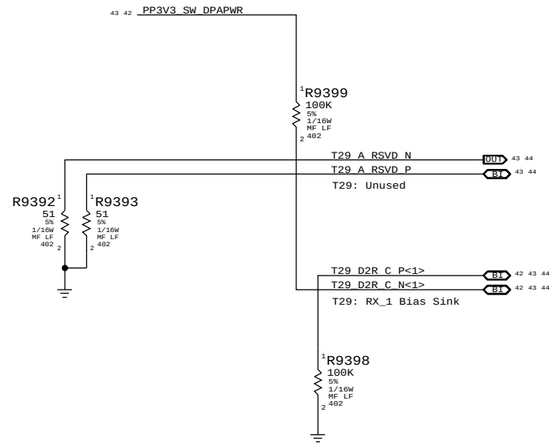
T29 A High-Speed Signals

T29 signals are
P/N-swapped after AC
caps to improve layout.



Port A MCU





SYNC_MASTER=T29_D	SYNC_DATE=11/01/2010
PAGE TITLE	T29 A PORT MICROCONTROLLER
Apple Inc.	DRAWING NUMBER 051-8774 · SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 93 OF 110
	SHEET 42 OF 48

Port A HV Power Switch

	Nominal	Min	Max
IFLT	2A	1.8A	2.2A
ILIM	829mA	687mA	971mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance @ 210K per TI

=PPHV_SW_DPAPWRSW
20V Max

U9410 SN1010017 QFN

IFLT = 200k / RFLT = 2A
ILIM = 201k / RLIM = 829mA +/- 142mA
TFLT = CCT * 38900
TSD = CCT * 100000

For 12V systems:
ILIM = 201k / RLIM = 1033mA +/- 156mA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0434	1	RES MTL FILM 1/16W 174K 1 0402 SMD LF	R9411		T29HV:P12V

	Nominal	Min	Max
ILIM	1033mA	877mA	1190mA, tolerance @ 174K per TI

3.3V/HV Power MUX

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

Blocking FET, off when
Source >3.4V or HV_EN high.

3.3V/HV MUXed

3.3V Always

Bleeder Resistor

2.5V / 249 ohm = 10mA
P = ~27mW

Note: Bleeder active when T29_A_HV_EN is LOW and DPAPWRSW_P3V3_ON_L is HIGH (>0.8V).

Port A 3.3V Power Switch

DP_PWR must be S4 to support wake from T29 devices.

U9480 TPS2051B SOT23

U9435 ZXRE060A SOT353

STOP_LEAK

DisplayPort/T29 A Connector

J9400 MDP-J59 F-ANG-TH

SHIELD PINS

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

T29: Unused

T29: TX_0

T29: LSX_R2P/P2R (P/N)

T29: TX_1

470k R's for ESD protection on AC-coupled signals.

SYNC MASTER=MASTER	SYNC DATE=N/A
PAGE TITLE	DisplayPort/T29 A Connector
Apple Inc.	DRAWING NUMBER 051-8774 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 94 OF 110
	SHEET 43 OF 48

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
PCIEG2 85D	*	N	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
PCIEG2 85D	TOP BOTTOM	Y	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF
CLK PCIE 90D	*	90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X DIELECTRIC	?
PCIEG2	*	=3X DIELECTRIC	?
CLK PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP BOTTOM	=4X DIELECTRIC	?
PCIEG2	TOP BOTTOM	=4X DIELECTRIC	?

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
I2C 55SE	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	0 1MM	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
I2C	*	=2x DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29 SPI 55S	*	=55 OHM SE	=55 OHM SE	=55 OHM SE	=55 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29 SPI	*	=2x DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP 90D	*	N	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF
T29DP 90D	TOP BOTTOM	Y	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DP CONNECTOR SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP 90D	*	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=4 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP BOTTOM	=4 1 SPACING	?

T29 Net Properties

T29 DP AND DOWNSTREAM PORTS

T29/DP TETHERED CABLE

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
PCIE CLK100M T29	CLK PCIE 90D	CLK PCIE	PCIE CLK100M T29 P	22 23
PCIE CLK100M T29	CLK PCIE 90D	CLK PCIE	PCIE CLK100M T29 N	22 23
	I2C 55SE	I2C	I2C T29 SCL	23 35
	I2C 55SE	I2C	I2C T29 SDA	23 35
T29 SPI CLK	T29 SPI 55S	T29 SPI	T29 SPI CLK	23
T29 SPI MOSI	T29 SPI 55S	T29 SPI	T29 SPI MOSI	23
T29 SPI MISO	T29 SPI 55S	T29 SPI	T29 SPI MISO	23
T29 SPI CS L	T29 SPI 55S	T29 SPI	T29 SPI CS L	23
	T29DP 90D	T29DP	T29 R2D C P<3..0>	23 42
	T29DP 90D	T29DP	T29 R2D C N<3..0> BEAD PROBE TRUE	23 42
	T29DP 90D	T29DP	T29 D2R P<3..0> BEAD PROBE TRUE	23 42
	T29DP 90D	T29DP	T29 D2R N<3..0> BEAD PROBE TRUE	23 42
T29 R2D0	T29DP 90D	T29DP	T29 R2D P<0> BEAD PROBE TRUE	42 43
T29 R2D0	T29DP 90D	T29DP	T29 R2D N<0> BEAD PROBE TRUE	42 43
T29 R2D1	T29DP 90D	T29DP	T29 R2D P<1> BEAD PROBE TRUE	42 43
T29 R2D1	T29DP 90D	T29DP	T29 R2D N<1> BEAD PROBE TRUE	42 43
	T29DP 90D	T29DP	T29 R2D C F P<1..0> BEAD PROBE TRUE	42
	T29DP 90D	T29DP	T29 R2D C F N<1..0> BEAD PROBE TRUE	42
T29 D2R0	T29DP 90D	T29DP	T29 D2R C P<0> BEAD PROBE TRUE	42 43
T29 D2R0	T29DP 90D	T29DP	T29 D2R C N<0> BEAD PROBE TRUE	42 43
T29 D2R1	T29DP 90D	T29DP	T29 D2R C P<1> BEAD PROBE TRUE	42 43
T29 D2R1	T29DP 90D	T29DP	T29 D2R C N<1> BEAD PROBE TRUE	42 43
	DP 90D	DISPLAYPORT	T29DPA ML P<1>	42 43
	DP 90D	DISPLAYPORT	T29DPA ML N<1>	42 43
	USB2 90D	USB2	T29 A RSVD P	42 43
	USB2 90D	USB2	T29 A RSVD N	42 43
	T29DP 90D	T29DP	T29 R2C P<1..0> BEAD PROBE TRUE	41
	T29DP 90D	T29DP	T29 R2C N<1..0> BEAD PROBE TRUE	41
T29 R2C0	T29DP 90D	T29DP	T29 R2C C P<0> BEAD PROBE TRUE	23 41
T29 R2C0	T29DP 90D	T29DP	T29 R2C C N<0> BEAD PROBE TRUE	23 41
T29 R2C1	T29DP 90D	T29DP	T29 R2C C P<1> BEAD PROBE TRUE	23 41
T29 R2C1	T29DP 90D	T29DP	T29 R2C C N<1> BEAD PROBE TRUE	23 41
T29 C2R0	T29DP 90D	T29DP	T29 C2R P<0> BEAD PROBE TRUE	23 41
T29 C2R0	T29DP 90D	T29DP	T29 C2R N<0> BEAD PROBE TRUE	23 41
T29 C2R1	T29DP 90D	T29DP	T29 C2R P<1> BEAD PROBE TRUE	23 41
T29 C2R1	T29DP 90D	T29DP	T29 C2R N<1> BEAD PROBE TRUE	23 41
	T29DP 90D	T29DP	T29 C2R C P<1..0> BEAD PROBE TRUE	41
	T29DP 90D	T29DP	T29 C2R C N<1..0> BEAD PROBE TRUE	41

INTERNAL PANEL PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
T366	DP 90D	DISPLAYPORT	DP INT ML C P<3..0>	7
T367	DP 90D	DISPLAYPORT	DP INT ML C N<3..0>	7
T368 DP_INT_ML	DP 90D	DISPLAYPORT	DP INT ML P<3..0>	7 21 48
T369 DP_INT_ML	DP 90D	DISPLAYPORT	DP INT ML N<3..0>	7 21 48
T371	DP 90D	DISPLAYPORT	DP INT AUXCH C P	7
T370	DP 90D	DISPLAYPORT	DP INT AUXCH C N	7
T372 DP_INT_AUXCH	DP 90D	DISPLAYPORT	DP INT AUXCH P	7 21 48
T373 DP_INT_AUXCH	DP 90D	DISPLAYPORT	DP INT AUXCH N	7 21 48

SYNC_MASTER=TONY SYNC_DATE=11/17/2010

PAGE TITLE: CONSTRAINTS: T29

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

REVISION C.0.0

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PAGE 100 OF 110

SHEET 44 OF 48

Temp Sensor Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMPSNS PAIR	*	55 OHM SE	=55 OHM SE	=55 OHM SE	20MM	0 25MM	0 10MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMPSNS	*	=2x DIELECTRIC	?

Temp Sensor Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING		
I420	TMPSNS_PAIR	TMPSNS	DX1_P	8
I421	TMPSNS_PAIR	TMPSNS	DX1_N	8
I422	TMPSNS_PAIR	TMPSNS	TDX1_P	8 48
I423	TMPSNS_PAIR	TMPSNS	TDX1_N	8 48
I429	TMPSNS_PAIR	TMPSNS	DX2_P	8
I431	TMPSNS_PAIR	TMPSNS	DX2_N	8
I430	TMPSNS_PAIR	TMPSNS	TDX2_P	8 48
I428	TMPSNS_PAIR	TMPSNS	TDX2_N	8 48

Temp sensor routes

AUDIO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0 6 MM	0 2 MM	10 MM	0 2 MM	0 2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0 2 MM	?

AUDIO NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING		
I448	AUDIODIFF	AUDIO	AUD_LTWT_N	15
I449	AUDIODIFF	AUDIO	AUD_LTWT_P	15
I450	AUDIODIFF	AUDIO	AUD_LWFR_N	15
I451	AUDIODIFF	AUDIO	AUD_LWFR_P	15
I452	AUDIODIFF	AUDIO	AUD_RTWT_N	16
I453	AUDIODIFF	AUDIO	AUD_RTWT_P	16
I454	AUDIODIFF	AUDIO	AUD_RWFR_N	16
I455	AUDIODIFF	AUDIO	AUD_RWFR_P	16
I456	AUDIODIFF	AUDIO	AUD_SUB_N	17
I457	AUDIODIFF	AUDIO	AUD_SUB_P	17

SPEAKER NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING		
I458	AUDIODIFF	AUDIO	SPKRAMP_LTWT_OUT_N	15 18 48
I459	AUDIODIFF	AUDIO	SPKRAMP_LTWT_OUT_P	15 18 48
I460	AUDIODIFF	AUDIO	SPKRAMP_LWFR_OUT_N	15 18 48
I461	AUDIODIFF	AUDIO	SPKRAMP_LWFR_OUT_P	15 18 48
I462	AUDIODIFF	AUDIO	SPKRAMP_RTWT_OUT_N	16 18 48
I463	AUDIODIFF	AUDIO	SPKRAMP_RTWT_OUT_P	16 18 48
I464	AUDIODIFF	AUDIO	SPKRAMP_RWFR_OUT_N	16 18 48
I465	AUDIODIFF	AUDIO	SPKRAMP_RWFR_OUT_P	16 18 48
I466	AUDIODIFF	AUDIO	SPKRAMP_SUB_OUT_N	17 18 48
I467	AUDIODIFF	AUDIO	SPKRAMP_SUB_OUT_P	17 18 48

I2C Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING		
	I2C_5SSE	I2C	I2C_LPCREM_SDA	20 21
	I2C_5SSE	I2C	I2C_LPCREM_SCL	20 21
	I2C_5SSE	I2C	DDC_SDA_FC	21 48
	I2C_5SSE	I2C	DDC_SCL_FC	21 48
	I2C_5SSE	I2C	SDA_FC	21 48
	I2C_5SSE	I2C	SCL_FC	21 48
	I2C_5SSE	I2C	SDA_SWREM	21
	I2C_5SSE	I2C	SCL_SWREM	21
	I2C_5SSE	I2C	I2C_DP628_SDA	35
	I2C_5SSE	I2C	I2C_DP628_SCL	35
	I2C_5SSE	I2C	I2C_LPCLOC_SDA	20 35
	I2C_5SSE	I2C	I2C_LPCLOC_SCL	20 35
	I2C_5SSE	I2C	I2C_FALS_SDA	10
	I2C_5SSE	I2C	I2C_FALS_SCL	10
	I2C_5SSE	I2C	I2C_LPC1_SDA	35
	I2C_5SSE	I2C	I2C_LPC1_SCL	35
	I2C_5SSE	I2C	I2C_ALS_SCL	35 48
	I2C_5SSE	I2C	I2C_ALS_SDA	35 48
	I2C_5SSE	I2C	I2C_USBHOST_SCL	35
	I2C_5SSE	I2C	I2C_USBHOST_SDA	35
	I2C_5SSE	I2C	ADAV4601_I2C_SDA	14
	I2C_5SSE	I2C	ADAV4601_I2C_SCL	14
	I2C_5SSE	I2C	I2C_SDA	12 14 18
	I2C_5SSE	I2C	I2C_SCL	12 14 18
	I2C_5SSE	I2C	AUD_161_I2C_SDA	12
	I2C_5SSE	I2C	AUD_161_I2C_SCL	12
	I2C_5SSE	I2C	I2C_MCU_SCL	34 35 42
	I2C_5SSE	I2C	I2C_MCU_SDA	34 35 42

I2C pairs from LPC

Audio I2C pairs

MicroCtlr Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING		
	MICROCTLR_5SSE	MICROCTLR	ADC_STR0_V	9 20
	MICROCTLR_5SSE	MICROCTLR	ADC_STR1_V	9 20
	MICROCTLR_5SSE	MICROCTLR	ADC_STR2_V	9 20
	MICROCTLR_5SSE	MICROCTLR	DAC_OUT	9 20
	MICROCTLR_5SSE	MICROCTLR	ADC_USB5V	20 33
	MICROCTLR_5SSE	MICROCTLR	P5VP3V3_VREF	9 39

SYNC_MASTER=TONY SYNC_DATE=11/17/2010

PAGE TITLE: CONSTRAINTS: AUDIO & MISC

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 103 OF 110

SHEET: 45 OF 48

Ethernet MDI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET MDI 100D	*	100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF	=100 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

PCIe Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING	
H17	PCIE_85D	PCIE	PCIE_ENET_R2D_P 26
H18	PCIE_85D	PCIE	PCIE_ENET_R2D_N 26
H19 PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P 7 26
H20 PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N 7 26
H21 PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P 7 26
H22 PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N 7 26
H23	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P 26
H24	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N 26
H25 PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P 22 26
H26 PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N 22 26

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW 110D	*	110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF	=110 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW TP	*	=3 1 SPACING	?

FIREWIRE PCIE NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING	
	PCIE_85D	PCIE	PCIE_FW_R2D_P 28
	PCIE_85D	PCIE	PCIE_FW_R2D_N 28
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P 7 28
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_N 7 28
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P 7 28
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_N 7 28
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P 28
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N 28
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P 22 28
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N 22 28

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2 90D	*	90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF	=90 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4 1 SPACING	?

USB PCIE NET PROPERTIES

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING	
	PCIE2_85D	PCIE2	PCIE_USB_D2R_C_P 32
	PCIE2_85D	PCIE2	PCIE_USB_D2R_C_N 32
	PCIE2_85D	PCIE2	PCIE_USB_R2D_P 32
	PCIE2_85D	PCIE2	PCIE_USB_R2D_N 32
PCIE_USB_R2D	PCIE2_85D	PCIE2	PCIE_USB_R2D_C_P 7 32
PCIE_USB_R2D	PCIE2_85D	PCIE2	PCIE_USB_R2D_C_N 7 32
PCIE_USB_D2R	PCIE2_85D	PCIE2	PCIE_USB_D2R_P 7 32
PCIE_USB_D2R	PCIE2_85D	PCIE2	PCIE_USB_D2R_N 7 32
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_USB_P 7 32
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_USB_N 7 32
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_USB_C_P 32
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_USB_C_N 32

Ethernet MDI Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING	
H25 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENETCONN_MDI_P<3..0> 26 27
H27 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENETCONN_MDI_N<3..0> 26 27
H30	ENET_MDI_100D	ENET_MDI	ENETCONN_MDI_T_P<3..0> 27
H29	ENET_MDI_100D	ENET_MDI	ENETCONN_MDI_T_N<3..0> 27

FireWire Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING	
FW_P0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P 29 30
FW_P0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_N 29 30
FW_P0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P 29 30
FW_P0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_N 29 30

USB Net Properties

	ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	SPACING	
USB UPSTREAM		USB2_90D	USB2	USB_HUB_UP_DP 31
		USB2_90D	USB2	USB_HUB_UP_DM 31
		USB2_90D	USB2	USB_DEV_DP 31
		USB2_90D	USB2	USB_DEV_DM 31
		USB2_90D	USB2	USB_DEV_F_DP 31
		USB2_90D	USB2	USB_DEV_F_DM 31
		USB2_90D	USB2	USB_HOST_DP 31 32
		USB2_90D	USB2	USB_HOST_DM 31 32
USB Hub ports		USB2_90D	USB2	USBDN1_H1_DP 31 33
		USB2_90D	USB2	USBDN1_H1_DM 31 33
		USB2_90D	USB2	USBDN2_H1_DP 31 33
		USB2_90D	USB2	USBDN2_H1_DM 31 33
		USB2_90D	USB2	USBDN3_H1_DP 31 33
		USB2_90D	USB2	USBDN3_H1_DM 31 33
		USB2_90D	USB2	USB_UC_DP 20 31
		USB2_90D	USB2	USB_UC_DM 20 31
		USB2_90D	USB2	USB_AUDIO_DP 11 31
		USB2_90D	USB2	USB_AUDIO_DM 11 31
		USB2_90D	USB2	USB_CAMERA_DP 10 31
		USB2_90D	USB2	USB_CAMERA_DM 10 31
		USB2_90D	USB2	CAM_DP 10 48
		USB2_90D	USB2	CAM_DM 10 48
USB AUDIO		USB2_90D	USB2	AUD_161_USB_DP 12
		USB2_90D	USB2	AUD_161_USB_DM 12
USB connector routes		USB2_90D	USB2	DM1 33
		USB2_90D	USB2	DP1 33
		USB2_90D	USB2	DM2 33
		USB2_90D	USB2	DP2 33
		USB2_90D	USB2	DM3 33
		USB2_90D	USB2	DP3 33

SYNC_MASTER=TONY SYNC_DATE=11/17/2010

PAGE TITLE
CONSTRAINTS:ENET, FIREWIRE & USB

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 105 OF 110
SHEET 46 OF 48

T29 Dr.B-Specific Physical & Spacing Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP ISL2 ISL3 ISL4 ISL5 ISL6 ISL7 BOTTOM	NO TYPE	MM	15 7

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55 OHM SE	=55 OHM SE	6 35 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55 OHM SE	*	Y	0 076 MM	0 076 MM	=STANDARD	=STANDARD	=STANDARD
55 OHM SE	TOP BOTTOM	Y	0 085 MM	0 085 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80 OHM DIFF	ISL3 ISL6	Y	0 120 MM	0 120 MM		0 150 MM	0 150 MM
80 OHM DIFF	TOP BOTTOM	Y	0 135 MM	0 135 MM		0 160 MM	0 160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85 OHM DIFF	ISL3 ISL6	Y	0 115 MM	0 115 MM		0 200 MM	0 200 MM
85 OHM DIFF	TOP BOTTOM	Y	0 125 MM	0 125 MM		0 200 MM	0 200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90 OHM DIFF	ISL3 ISL6	Y	0 099 MM	0 099 MM		0 200 MM	0 200 MM
90 OHM DIFF	TOP BOTTOM	Y	0 099 MM	0 099 MM		0 150 MM	0 150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100 OHM DIFF	ISL3 ISL6	Y	0 081 MM	0 081 MM		0 250 MM	0 250 MM
100 OHM DIFF	TOP BOTTOM	Y	0 091 MM	0 091 MM		0 250 MM	0 250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110 OHM DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110 OHM DIFF	ISL3 ISL6	Y	0 067 MM	0 067 MM		0 300 MM	0 300 MM
110 OHM DIFF	TOP BOTTOM	Y	0 075 MM	0 075 MM		0 300 MM	0 300 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1 1 DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0 1 MM	0 1 MM

Standard Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0 1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1 1 SPACING	*	0 1 MM	?
2 1 SPACING	*	0 2 MM	?
3 1 SPACING	*	0 3 MM	?
4 1 SPACING	*	0 4 MM	?
5 1 SPACING	*	0 5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X DIELECTRIC	TOP BOTTOM	0 140 MM	?
3X DIELECTRIC	TOP BOTTOM	0 210 MM	?
4X DIELECTRIC	TOP BOTTOM	0 280 MM	?
5X DIELECTRIC	TOP BOTTOM	0 355 MM	?
2X DIELECTRIC	*	0 152 MM	?
3X DIELECTRIC	*	0 228 MM	?
4X DIELECTRIC	*	0 304 MM	?
5X DIELECTRIC	*	0 380 MM	?

SYNC_MASTER=TONY SYNC_DATE=11/17/2010

PAGE TITLE: T29 PCB Rule Definitions

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 109 OF 110

SHEET: 47 OF 48

FUNCTIONAL TEST POINTS

J1013 ODD FAN

8	IN	FAN0_PWR	FUNC_TEST_TRUE
8	IN	FAN_TACH0	FUNC_TEST_TRUE
19	IN	PP12V_FAN_FET	FUNC_TEST=TRUE MIN ALLOWED TPS=3

3 GROUND TESTPOINTS NEAR J1013

J1115 BLC CONNECTOR

9	IN	STR0_+	FUNC_TEST_TRUE
9	IN	STR0_-	FUNC_TEST_TRUE
9	IN	STR0C	FUNC_TEST_TRUE
9	IN	STR1_+	FUNC_TEST=TRUE
9	IN	STR1_-	FUNC_TEST_TRUE
9	IN	STR1C	FUNC_TEST_TRUE
9	IN	STR2_+	FUNC_TEST_TRUE
9	IN	STR2_-	FUNC_TEST_TRUE
9	IN	STR2C	FUNC_TEST_TRUE

2 GROUND TESTPOINTS NEAR J1013

J1204 USB CAMERA

10	IN	PP5V_CAM_FILT	FUNC_TEST_TRUE MIN ALLOWED TPS=1
46 10	IN	CAM_DM	FUNC_TEST=TRUE
46 10	IN	CAM_DP	FUNC_TEST=TRUE
45 35	IN	I2C_ALS_SCL	FUNC_TEST=TRUE
45 35	IN	I2C_ALS_SDA	FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J1204

J2007 MICROPHONE

18	IN	AUD_MIC_IN_N_CONN	FUNC_TEST_TRUE
18	IN	GND_AUD_MIC_CONN	FUNC_TEST=TRUE
18	IN	AUD_MIC_IN_P_CONN	FUNC_TEST=TRUE

2 GROUND TESTPOINTS NEAR J2007

J2003 AUDIO LEFT SPEAKER

45 18 15	IN	SPKRAMP_LWFR_OUT_P	FUNC_TEST_TRUE
45 18 15	IN	SPKRAMP_LWFR_OUT_N	FUNC_TEST_TRUE
45 18 15	IN	SPKRAMP_LTWT_OUT_P	FUNC_TEST_TRUE
45 18 15	IN	SPKRAMP_LTWT_OUT_N	FUNC_TEST_TRUE

J2004 AUDIO RIGHT SPEAKER

45 18 16	IN	SPKRAMP_RWFR_OUT_P	FUNC_TEST=TRUE
45 18 16	IN	SPKRAMP_RWFR_OUT_N	FUNC_TEST=TRUE
45 18 16	IN	SPKRAMP_RTWT_OUT_P	FUNC_TEST=TRUE
45 18 16	IN	SPKRAMP_RTWT_OUT_N	FUNC_TEST=TRUE

J2005 AUDIO SUBWOOFER

45 18 17	IN	SPKRAMP_SUB_OUT_P	FUNC_TEST=TRUE
45 18 17	IN	SPKRAMP_SUB_OUT_N	FUNC_TEST=TRUE
18 17 16 15 13	IN	GND_AUDIO_SPKRAMP	FUNC_TEST_TRUE MIN ALLOWED TPS=6

J1011 BLOWER TEMP SENSOR

45 8	IN	TDX1_N	FUNC_TEST=TRUE
45 8	IN	TDX1_P	FUNC_TEST=TRUE

2 GROUND TESTPOINTS NEAR J1011

J1012 PSU TEMP SENSOR

45 8	IN	TDX2_N	FUNC_TEST_TRUE
45 8	IN	TDX2_P	FUNC_TEST_TRUE

2 GROUND TESTPOINTS NEAR J1012

J2726 PANEL POWER

21	IN	PP12V_PANEL_FC	FUNC_TEST_TRUE MIN ALLOWED TPS=4

4 GROUND TESTPOINTS NEAR J2726

J2725 INTERNAL DP PANEL

44 21 7	IN	DP_INT_ML_P<3..0>	FUNC_TEST=TRUE
44 21 7	IN	DP_INT_ML_N<3..0>	FUNC_TEST=TRUE
44 21 7	IN	DP_INT_AUXCH_P	FUNC_TEST_TRUE
44 21 7	IN	DP_INT_AUXCH_N	FUNC_TEST=TRUE
45 21	IN	DDC_SCL_FC	FUNC_TEST=TRUE
45 21	IN	DDC_SDA_FC	FUNC_TEST=TRUE
45 21	IN	SCL_FC	FUNC_TEST=TRUE
45 21	IN	SDA_FC	FUNC_TEST=TRUE
21	IN	AUDIO_ON_FC	FUNC_TEST=TRUE
21	IN	AUDIO_MUTE_FC_L	FUNC_TEST_TRUE
21	IN	I2S_SCLK_FC	FUNC_TEST=TRUE
21	IN	I2S_WS_FC	FUNC_TEST=TRUE
21	IN	I2S_SD0_FC	FUNC_TEST=TRUE
21	IN	DP_PWR_UP_FC	FUNC_TEST=TRUE
21	IN	INT_FC_L	FUNC_TEST=TRUE
21	IN	DP_INT_HPD_FC	FUNC_TEST=TRUE
21	IN	VIDEO_ON_FC	FUNC_TEST=TRUE
21	IN	VSYNC_FC	FUNC_TEST=TRUE

17 GROUND TESTPOINTS NEAR J2725

GND		36 TP'S	FUNC_TEST_TRUE MIN ALLOWED TPS=36

NC AND NO_TEST NETS

FLIP SIDE PCI BRIDGE AND USB CONTROLLER MOUNTING AND ROUTING MAKES TEST VIRTUALLY IMPOSSIBLE

TP_PCIBR_WAKE_L	NC_PCIBR_WAKE_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_EECS_L	NC_PEX8112_EECS_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_EECLK	NC_PEX8112_EECLK	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_EERDDATA	NC_PEX8112_EERDDATA	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_EEWRDATA	NC_PEX8112_EEWRDATA	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GPIO0	NC_PEX8112_GPIO0	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GPIO1	NC_PEX8112_GPIO1	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GPIO2	NC_PEX8112_GPIO2	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GPIO3	NC_PEX8112_GPIO3	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_PWR_OK	NC_PEX8112_PWR_OK	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_BAR0ENB_L	NC_PEX8112_BAR0ENB_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_PCLKO62SEL_L	NC_PEX8112_PCLKO62SEL_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_PMEOUT_L	NC_PEX8112_PMEOUT_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GNT1_L	NC_PEX8112_GNT1_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GNT2_L	NC_PEX8112_GNT2_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GNT3_L	NC_PEX8112_GNT3_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_PCLKO	NC_PEX8112_PCLKO	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_SMI_L	NC_NECUSB_SMI_L	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_PPON1	NC_NECUSB_PPON1	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_PPON2	NC_NECUSB_PPON2	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_PPON3	NC_NECUSB_PPON3	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_SRCLK	NC_NECUSB_SRCLK	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_SRDTA	NC_NECUSB_SRDTA	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_SRMOD	NC_NECUSB_SRMOD	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_TESTEN	NC_NECUSB_TESTEN	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_TEST3	NC_NECUSB_TEST3	MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_TEST4	NC_NECUSB_TEST4	MAKE_BASE=TRUE NO_TEST=TRUE

PCI_AD<31..0>	NO_TEST=TRUE
PCI_C_BE_L<3..0>	NO_TEST=TRUE
PCI_PAR	NO_TEST=TRUE
PCI_FRAME_L	NO_TEST=TRUE
PCI_IRDY_L	NO_TEST=TRUE
PCI_TRDY_L	NO_TEST=TRUE
PCI_DEVSEL_L	NO_TEST=TRUE
PCI_STOP_L	NO_TEST=TRUE
PCI_PERR_L	NO_TEST=TRUE
PCI_SERR_L	NO_TEST=TRUE
PCI_NECUSB_REQ_L	NO_TEST=TRUE
PCI_NECUSB_GNT_L	NO_TEST=TRUE
PCI_NECUSB_INT_L	NO_TEST=TRUE
PCI_CLKRUN_L	NO_TEST=TRUE
PCI_RESET_L	NO_TEST=TRUE

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: J59 ICT/FCT

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 110 OF 110

SHEET: 48 OF 48